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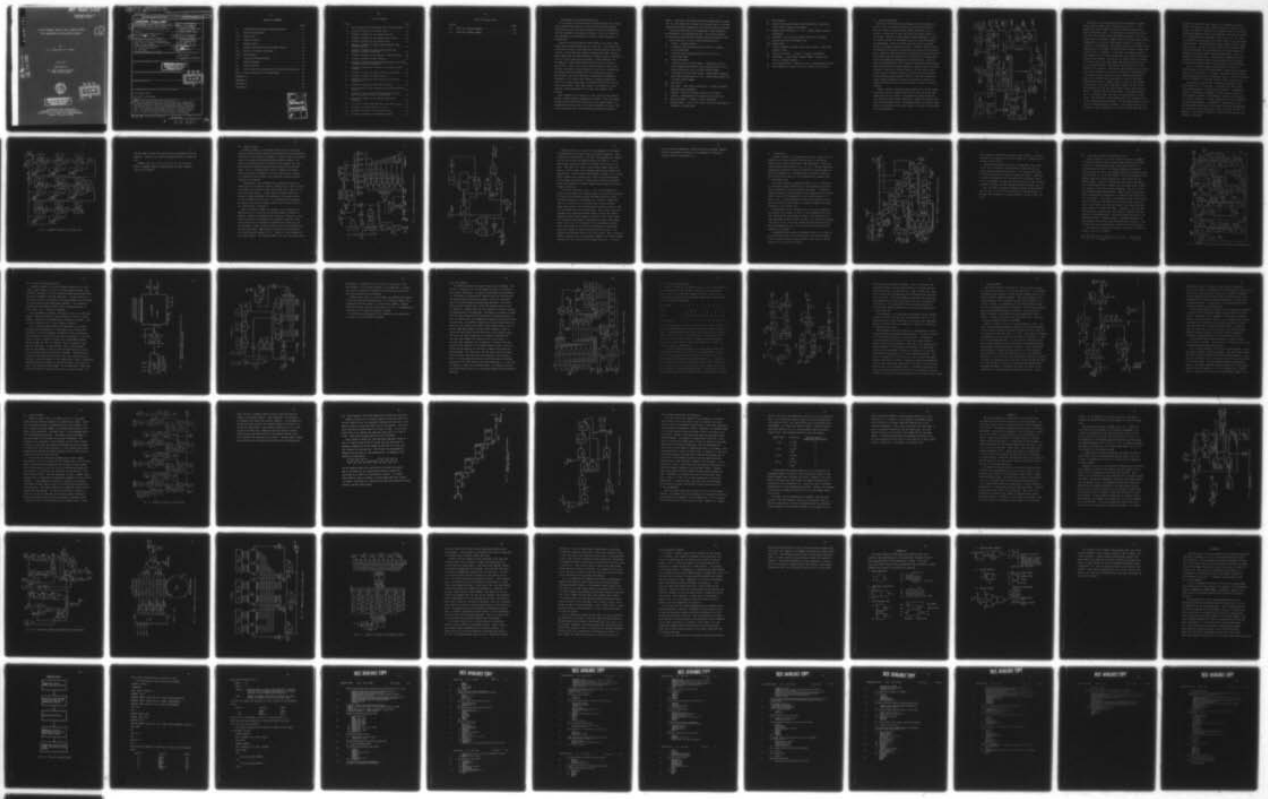

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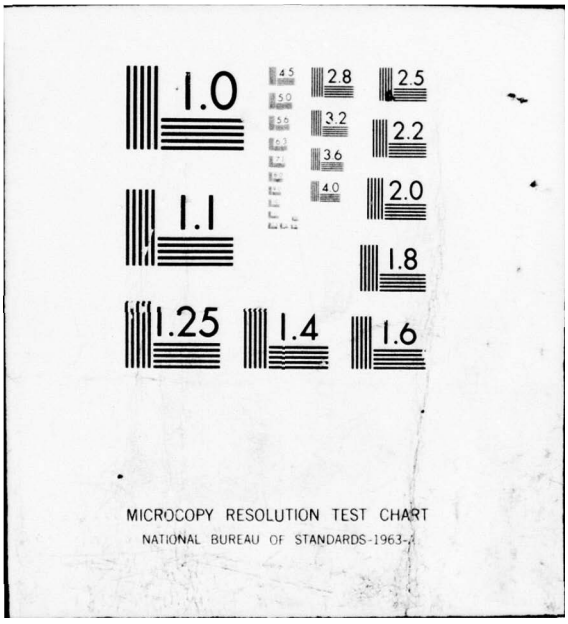
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A MULTI-CHANNEL DIGITAL DATA LOGGING SYSTEM FOR IONOSPHERIC SCINTILLATION STUDIES

(1)

by

K. S. Yang and A. L. Hearn

July 1977

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

In this report ~~we~~ describe a multi-channel digital data logging system designed specifically to digitize and record the analog transmissions from radio beacon satellites which are subsequently used for ionospheric scintillation studies. System specifications and design diagrams are given. This system has been actually built and is currently recording data. The computer software necessary to produce a digital magnetic tape for further data processing is described in the Appendix.

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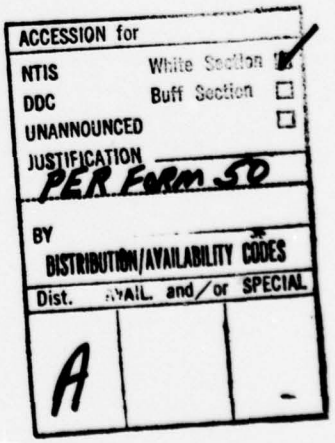

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I. Introduction and System Specifications

In this report we describe a multi-channel digital data logging system designed specifically to digitize and record the analog transmissions from radio beacon satellites which are subsequently used for ionospheric scintillation studies. Since the scintillation phenomena is time dependent, accurate timing information is recorded also.

Basically this data logging system accepts up to eight analog inputs which are multiplexed onto a single line. This single line is digitized to give a three BCD digit (000-999) parallel data word to which a single BCD digit channel identification and a two BCD digit frame count for timing purposes is added to form a 6 BCD digit (24 bit) word of useful data per sample. Eight additional bits are added as a frame identification which serves as a flag required later. This 32 bit word is shifted serially from a shift register to provide a single channel of serial data. Periodically, two header words are inserted into this serial data stream to provide data, time, and 5 BCD digits (selectable) of arbitrary information. This serial data stream is di-phase encoded such that only a single audio signal is required for both the data and timing clock pulses. This audio signal is recorded on a single track of a high performance reel to reel type magnetic tape recorder.

Also included in this system is a real time data verification scheme to assure accurate recording of the data. This is provided through the read after write provision on the tape recorder. The recorded data are sent back to the system, decoded to retrieve the original data and clock, and selectively displayed according to

channel. Similarly, the audio tape can be played back at a later date to allow packing of the data onto a digital tape in a format compatible with most computers for the final analysis of the data.

Detailed descriptions of the components of the system will be presented in the following sections. All digital controls are carried out with TTL logic modules [Morris and Miller, 1971].

The following is a list of system characteristics:

I. Inputs: 8 analog sources.

a) 4 channels with voltage range from +200 mv to +800 mv into 100,000 ohms.

b) 4 channels with voltage range from +1.0 v to 5.0 v into 10,000 ohms.

II. Analog Processing:

a) 4 channels with low level inputs: integrating for the entire sampling period with output ranging from 0 to +10 v before digitization into a 3-digit decimal number.

b) 4 channels with high level inputs: instantaneous sampling with output ranging from 0 to +10 v before digitization into a 3-digit decimal number.

III. Time Clock:

a) Time Base: 1 MHz crystal oscillator, $\pm$ 0.0025%, trimable. Buffered output available.

b) Display: Date, Hour, Minute, Second in 24^{h} format.

c) Control: synchronization of the second, and clock set.

IV. Data Clock Rate: 2.5 KHz, 5.0 KHz, selectable.

V. Sampling Rate: 1 Hz, 20 Hz, 50 Hz, or 100 Hz, selectable in automatic or manual mode.

VI. Data Display:

a) Digital--Pre-recorded data, post-recorded data, selectable. Single channel display, selectable.

b) Analog--Pre-integration, 0 - 10 v. Single channel display, selectable.

VII. Time Mark: Relay contact closure formatted for showing minutes and hours for external use.

VIII. Header Block:

a) 3-digit observation number, Date, Hour, Minute, 2-digit code number, in BCD.

b) *Insertion Interval: 1 Minute, 10 minute, selectable.*

IX. Data Block: 3-digit data, channel number, 2-digit frame count, in BCD per channel.

X. Data Stream Format: 6 BCD digits plus 2 frame identity digits.

XI. Power Required: +5VDC $\pm$ 2.5% @ 6A $\pm$ 15VDC $\pm$ 2.5% @ 0.5A.

II. System Organization

Except for the analog data processing and the interface with digital logics, functional controls are entirely built up with TTL logic chips of the SN74 family [Morris and Miller, 1971]. Layouts in groups more or less follow the functional pattern of the system. There are 3 large digital boards numbered I, II, and III, which hold most of the digital logics for the system timing and bookkeeping. Board I contains the time clock, its display drivers, and channel selection controls. Board II contains logics for generating the system clock and the serializing of the parallel data. Board III holds the logics for encoding the serial data prior to recording and also contains the receiver for the recorded data which are decoded and displayed on the control panel. Board IV holds the analog/digital (A/D) converter and the analog multiplexer which allows all the 8 analog channels to share the use of the same converter. There are 2 plug-in boards, V and VI, which serve as digital control interface between the analog processing circuits and the digital control system. Finally, there are 4 additional plug-in boards numbered VII through X containing 2 channels of analog processing circuits on each board for a total of 8 analog channels.

Figure 1 shows a functional block diagram of the entire system. Each block contains a numeral indicating on which board the associated circuits are located. Interconnections among blocks are also labeled to show control directions. Double-lined arrows indicate multi-connection lines. Unterminated boxes are controls available to the operator on the control panel to activate various modes of system operations.

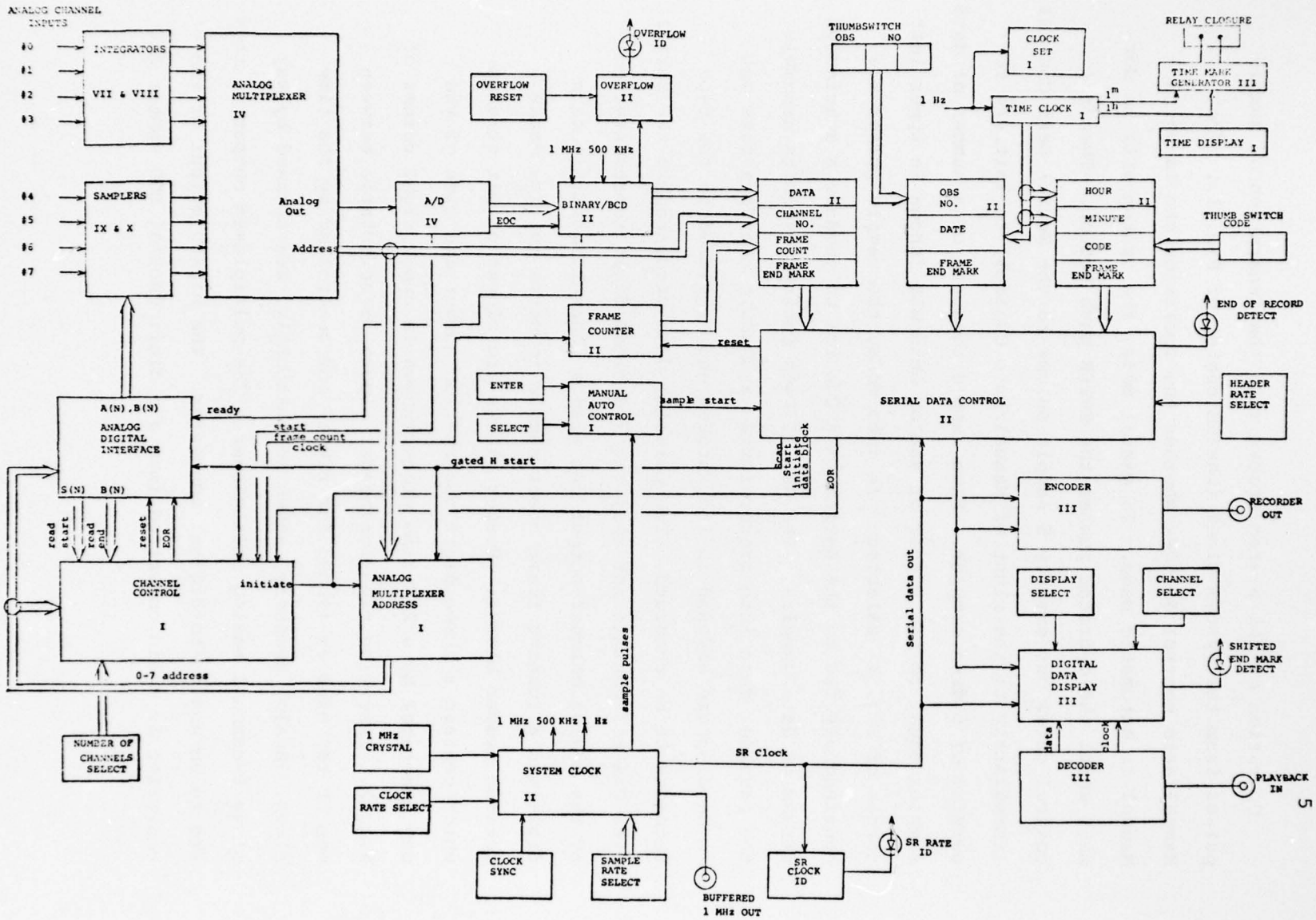


Fig. 1. Block diagram of an 8-channel data logging system.

Operation of the system starts with the generation of sample pulses from the System Clock (bottom center of Fig. 1). The Manual/Auto control decides whether the operation should be in Manual or Automatic mode. In manual mode, the system will be dormant until the operator pushes the ENTER push button. Then the control gates out exactly 5 sample pulses to the Serial Data Control (immediately to the right of Manual/Auto Control) to initiate recording of 5 data samples. Each sample consists of a number of data samples equal to the number of analog channels (shown in upper left corner of Fig. 1) selected. In auto mode, the sample pulses are continuously fed to the Serial Data Control to produce a continuous stream of data samples. The Serial Data Control circuits assemble the parallel data into proper format and shift the data bits out to be di-phase encoded in the Encoder and delivered to the tape recorder to be recorded. The parallel data presented to the Serial Data Control contain not only the 3 decimal digit representation of the analog channel output but also a channel identification digit and a running frame count number to serve as time marks between header blocks. Header blocks are blocks of bit streams which contain a three digit observation number and time of the day generated by a 24^h time clock (shown in upper right corner of Fig 1). Insertion rate for header blocks is selectable between one or ten minutes (shown far right) and controlled by the time clock. Analog channels, shown schematically, are scanned by way of an 8-channel analog multiplexer. The multiplexed output is then fed to an analog-to-digital converter. The binary output of the converter is again converted into a 3 digit decimal BCD number and

presented to the Serial Data Control to be assembled into data blocks. The Channel Control, shown in lower left portion of Fig. 1, selects the number of channels to be scanned by way of the Analog Multiplexer Address generator and coordinates the analog processing via the Analog/Digital Interface (center left of Fig. 1). There is a provision for displaying the 3 digit output of any particular analog channel. The Digital Data Display circuits shown on lower right of Fig. 1, selects either the serial data bit stream output (pre-recording data) or the decoded data bit stream through the playback of the tape recorder (post-recording data) to be displayed on the control panel. The Decoder is required since the recorded bit stream has been di-phase encoded before recording. The particular channel output to be displayed is also selectable.

For ease of signal tracing and servicing, the origins of control signals are given by coded numbers indicating their precise locations in the system. For example, the sample pulses originate from the System Clock block, situated on Board II, and can be located on pin 5 of module 19, thus the notation IIM19-5 as seen in Fig. 4.

In sections III through XII, detailed descriptions of each block shown in Fig. 1 are given. In section XIII, some limitations and advantages of the system are discussed. In Appendix A, another is described to complement the data logger so that the data stream as recorded on audio magnetic tape can be transfered to a digital tape deck in a format compatible with other computers for final data analysis. In Appendix B, several basic logic building blocks used often in the system are listed and explained for those who are not familiar with logic circuits. Finally, in Appendix C, the software necessary to unpack the digital tape just produced is described.

III. Time Clock

The clock is of the conventional type in the normal 24^h format using SN7490's as divide-by-ten counters for the 1 second and 1 minute digits and SN7492's as divide-by-six counters for the 10 second and 10 minute digits. The 1 Hz input to the clock is derived by direct count-down from a 1 MHz crystal controlled oscillator on the system clock board (board II). The AND gate M15-1,2,3 (Pins 1,2, and 3 of Module 15) provides the 24^h reset control and in addition increments the data count in the 3-digit date counters that follow. Except for the 1^s counter input, all subsequent inputs are EX-ORed with an AND-gated 1 Hz pulse through normally shorted push buttons. This scheme allows one to set each digit of the clock by advancing that digit at the rate of 1 Hz without interfering the normal clock advances that affects that particular digit. This allows the clock to be set at any instant without regard to the actual time registered by the clock; and more important, the clock will not lose synchronization if the input 1 Hz pulse has been synchronized ahead of time. By depressing the button under the 1 second digit, the 1 Hz pulse is gated out, this stops the advance of the clock and allows the true time to catch up with what is registered in the clock counters.

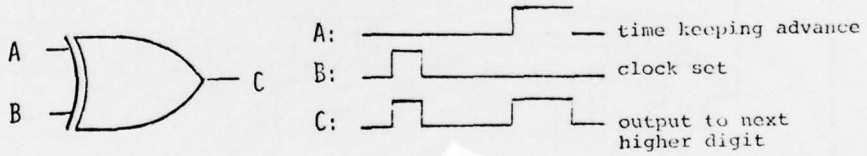
It should be noted that the advancing of a digit by this method also carries over to the next higher digit. Therefore, to avoid any unnecessary resetting, one should set the clock by beginning with the one second digit and proceeding on to higher order digits.

The contents of the clock are presented to corresponding 7-segment encoders for driving 7-segment LED display modules. They are also

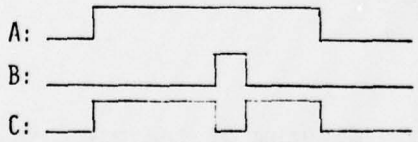
presented to the formatter (on board II) to be serialized when a header block has been called for.

Fig. 2 is the schematic for the clock proper. Input/output information carries the notation that will be the same throughout this report, e.g., IIM21-13 meaning (to/from) pin 13 of Module number 21 on board II.

Referring to Fig. 2, it is seen that the time keeping is accomplished by accumulating the 1 Hz pulses, generated from System Clock, IIM21-13, in the format of $999^{d}23^{h}59^{m}59^{s}$. Ripple counters (M20, 21, 22, 23, 29, 33, 32, 31, and 30), SN7490 , SN7492 are used for this purpose. As stated previously, the normal advancing of digits in keeping real time and the mechanism to set clock are shared through Exclusive-Or gates. This is to avoid exclusion of one against the other. Two possibilities in timing may arise, that is, during time-set, the time keeping advance may or may not be there. In the absence of time advance, the situation can be explained as follows:



During the normal time advance, the following case exists:



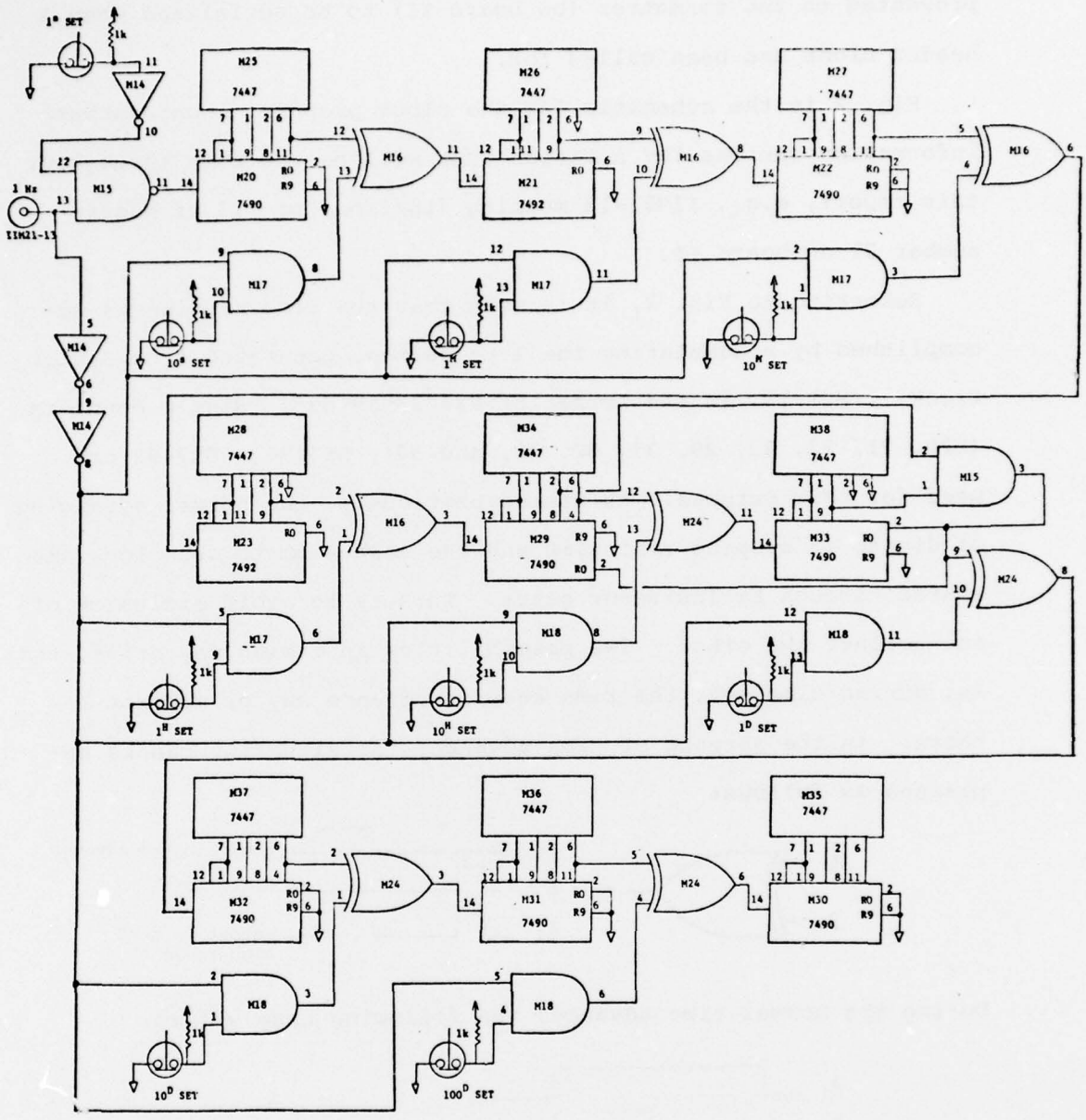


Fig. 2. Schematic diagram of the Time Clock

The net result is that the next digit will be advanced twice as required. Clearly this cannot be accomplished with a simple OR gate.

Modules, M25, 26, 27, 28, 34, 38, 37, 36, 35, are 4-bit BCD to 7 segment readout encoder/drivers for panel readouts. They are all SN7447's.

IV. Channel Control

Located on board I, the Channel Control circuit selects the number of analog channels desired and coordinates the analog/digital conversion of each channel accordingly. Figure 3 shows its schematic which also includes the analog multiplex address counter. The number of channels desired is selected by the operator on a normally shorted 8-station selector switch located on the control panel. Fig. 4, the Manual/Auto control, augments the channel control and makes it possible to initiate the start of a sample or a sequence of data blocks, with each block representing data contents of one channel.

In Manual mode, upon command from the operator through the "Manual Enter" push button, exactly 5 sample pulses, which initiate each sample, are allowed to pass (counter M8) and it stops at the end of the fifth sample. In Auto mode, the sample pulses are allowed to pass unhindered, thus producing a continuous record at the set sampling rate until it is terminated by the operator by returning the system to Manual mode without further action on the "Manual Enter" push button.

Upon initiating a sample, the channels to be digitized are addressed one at a time until the desired number of channels is reached. Channels are numbered from 0 through 7 requiring a 3-bit binary code which is generated by the address counter M9. NAND gates, M5 and M6, are designed to coordinate the timing for the A/D converter to start conversion and to initiate the sequence for the next data block. NAND gate M10 senses the end and gates out the initiate record command (Fig. 6 , IIM29-13), thus terminating the current sample. The sequence repeats with the next sample pulse.

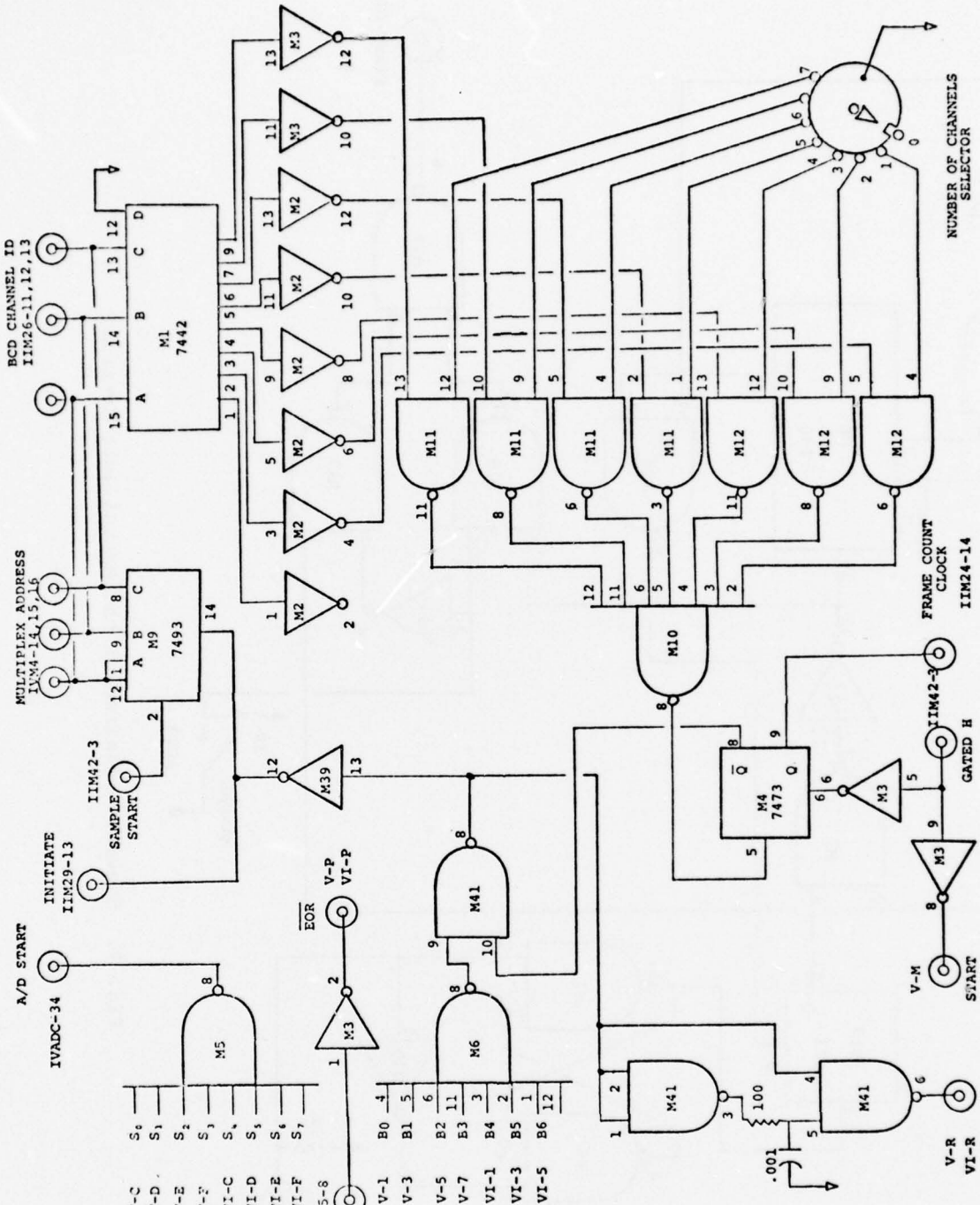


Fig. 3. Schematic diagram of the Channel Control

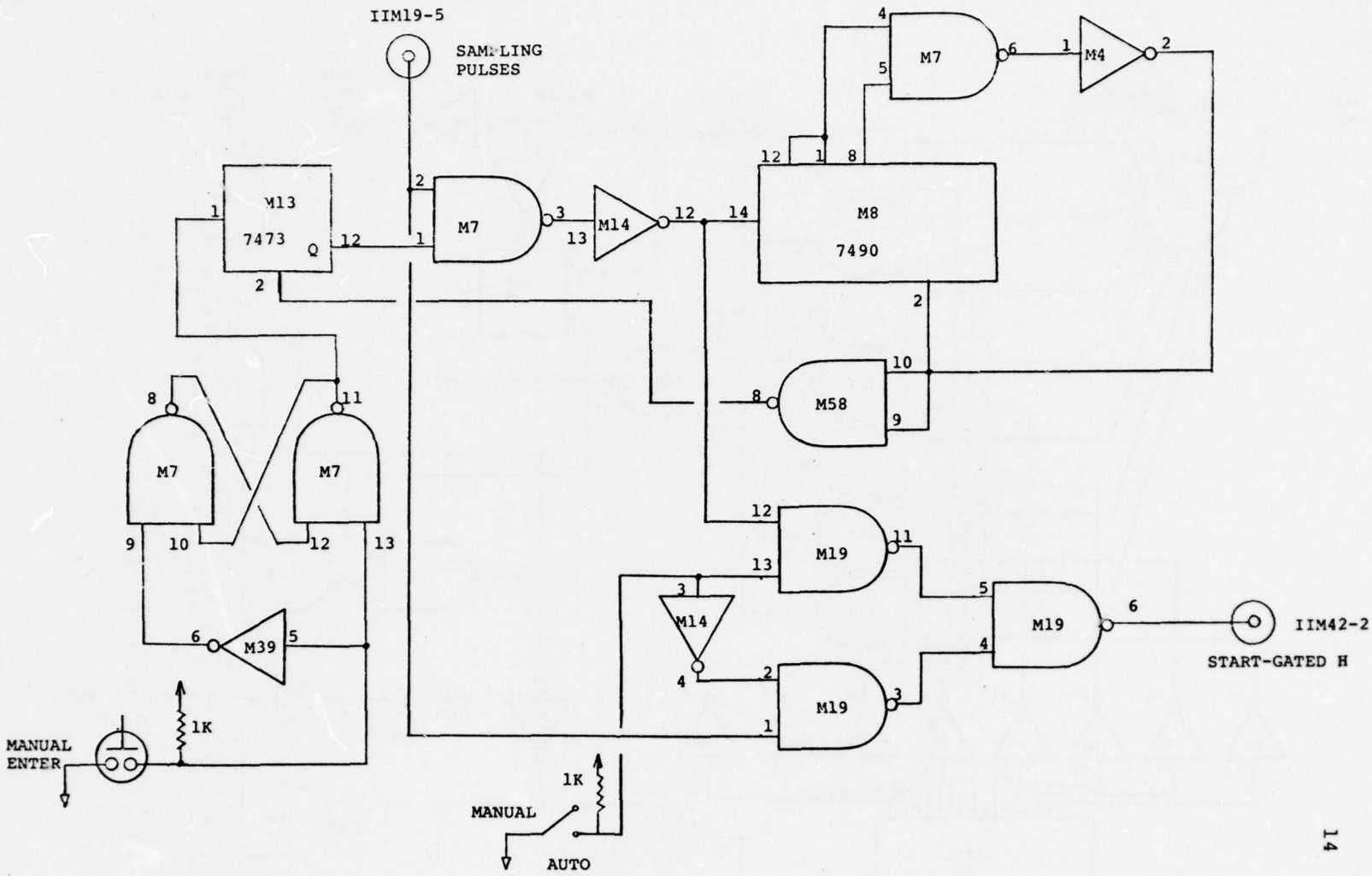


Fig. 4. Schematic diagram of the Manual/Auto Control.

Referring to Fig. 4, the R-S FF (see Appendix II) following the Manual Enter push button acts as a contact debouncer. Upon releasing the push button, J-K FF (M13) (see Appendix II) toggles and sets up to gate the sampling pulses from IIM19-5. In the Manual Mode, the switch shown in the lower center of Fig. 4 is open. Thus M19-13 is 'high' to allow manual sample pulses and M14-2 is 'low' to gate out the regular sample pulse streams (see Appendix II). Decade counter (M8, SN7490) is wired as a ÷5 scaler. M19-12 channels the 5 pulses out to start the system operation. In Auto mode, that switch is closed, which gates out the manual pulses and channels the regular sample pulses through the OR gate formed by M19-4,5,6.

On the left hand side of Fig. 3, the 2 8-input NAND gates serve as OR functions for signaling when one of the analog channels is ready to be digitized and when the READ process has ended. A trailing edge detector (see Appendix II) formed by 2 NAND gates (M41-1,2,3 and M41-4,5,6) and an RC delay circuit produces a sharp reset pulse to the Analog/Digital Interface circuit to turn off the channel that has just been read. The initiate pulse also increments the analog multiplexer address counter (M9, SN7493), readying the next analog channel to be read. The binary output of the counter also derives a BCD/decimal converter (M1, SN7442) which gives 1 out of 8 indications of the multiplexer address. After level adjusted, they serve as references for comparison against the number of channel selector switch settings. Comparators are formed by gates of M11, M12 and M10. When a selected channel coincides with the multiplexer address, J-K FF (M4) toggles and gates out the initiate pulse through M41-8,9,10. It should

be noted that the comparison is done after the multiplexer address has been incremented, therefore, it is necessary to offset the selector switch by bypassing ch. Ø.

V. System Clock

Located on board II, the system clock circuit, shown in Fig. 5, generates all timing pulses for various parts of the system. Starting with a crystal controlled 1 MHz oscillator, a series of ripple decade counters (M12, 13, 14, 15, 16, 17 and 42) synthesize frequencies required by the shift registers for serialization of data, the sampling rate, the binary data to BCD data converter, and the time clock, which in turn, generates the insertion rate for the header block.

The crystal, shown in upper left corner of Fig. 5, operating in the series resonant mode utilizes 2 self-biased TTL inverters (M5-1,2 and M5-3,4) to form the basic oscillator. A series adjustable capacitor allows trimming of the frequency to be accurate within 1 part in 10^8 although the X'tal is only rated for 2.5 parts in 10^5. A buffered output at TTL voltage levels is available at the back of the chassis to be used to compare with other standards or for external use.

Through gates on M11, the data shift rate can be selected by the operator to be either 2.5 KHz or 5 KHz consistent with eventual recording onto audio magnetic tapes. The sampling rate is also selectable by gates on M23, and M22 to be one of the following: 1 Hz, 20 Hz, 50 Hz, or 100 Hz, through selector switch on front panel and appropriate taps from the scaling counters that generates the 1 Hz signal.

The sampling rate pulses are delayed by about 6μs in order to give sufficient time to turn the data block off when the header block is being inserted, since otherwise, their relative timing prevents one to gate out the other.

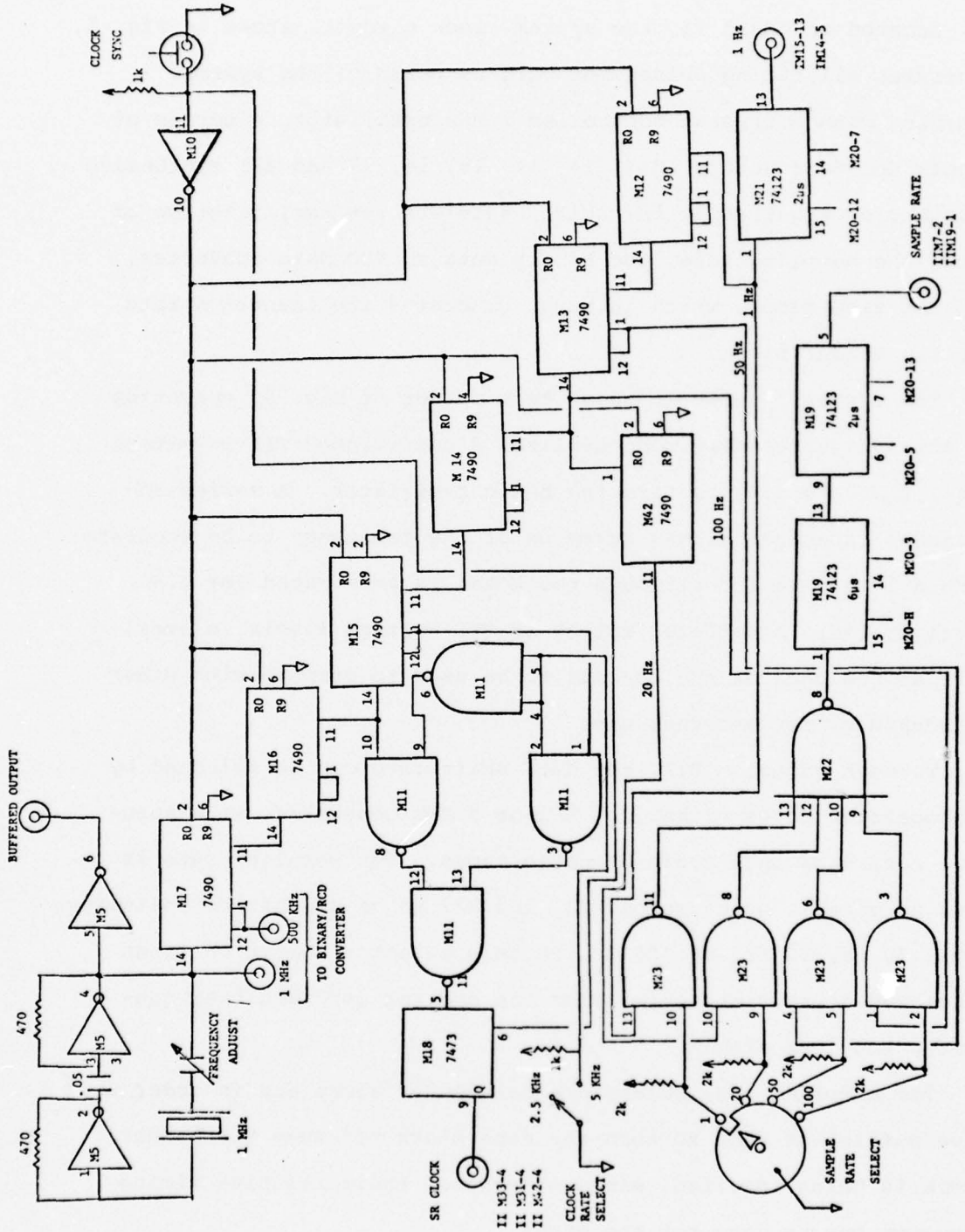


Fig. 5. Schematic diagram of the System Clock

This is done by cascading two one-shots (M19, SN74123). The first provides the 6μs delay and the second sends out 2μs sample pulse to the Serial Data Control.

A push button labeled "Clock Sync" (shown upper right corner of Fig. 5) is available to the operator to reset and stop the divider chain by holding the button in. All counters will start from zero count when the operator releases the button. Therefore, it serves to synchronize the 1 Hz pulse with an external timing tick if the operator releases the button upon hearing the 1^{s} ticks available on almost any time standard broadcast like WWV, CHU, etc.

The 1 Hz pulse is generated through 6 decade counters (SN7490) (M17, 16, 15, 14, 13 and 12) by scaling the 1 MHz oscillator. A one-shot (M21) produces a 2μs pulse before it is sent to the time clock.

VI. Serial Data Generator and Format Control

Located on board II, this unit, shown in Figure 6, assembles all pertinent parallel data bits into proper format and then upon receiving an initiate pulse (upper left corner, IM39-12), it serializes the data into a bit stream clocked by the selected rate of either 2.5 KHz or 5 KHz through parallel-in-serial-out shift registers (M28, 27, 26 and 25) SN74165. The data representing each channel forms a data block consisting of 3 BCD digits for the channel output, 1 digit to identify the channel and 2 BCD digits as a running frame count of frames since the header block in which the contents of the time clock are presented. This is to serve as time marks between header blocks. Each frame of record represents one sample point consisting of a number of data blocks, one for each channel. In addition, 2 hex-decimal digits (FC) are hard-wired (see M28) into the format to be used as a flag to mark the end of a data block since they are unique in the sense that they cannot appear in a normal BCD number. Detection of this end mark through serial-in-parallel-out shift register (SN74164, M34) and gates M35, called EOR (M35-8), initiates another data block if so required (see IM3-1, Channel Control). Successful detection of EOR indicates that the data have been shifted out correctly. This is shown by an LED indicator which flashes on the control panel.

The format of the data block stream, in the first in first out fashion, is given as follows:

800 400 200 100 80 40 20 10 8 4 2 1 — DATA

8 4 2 1 — CH. ID

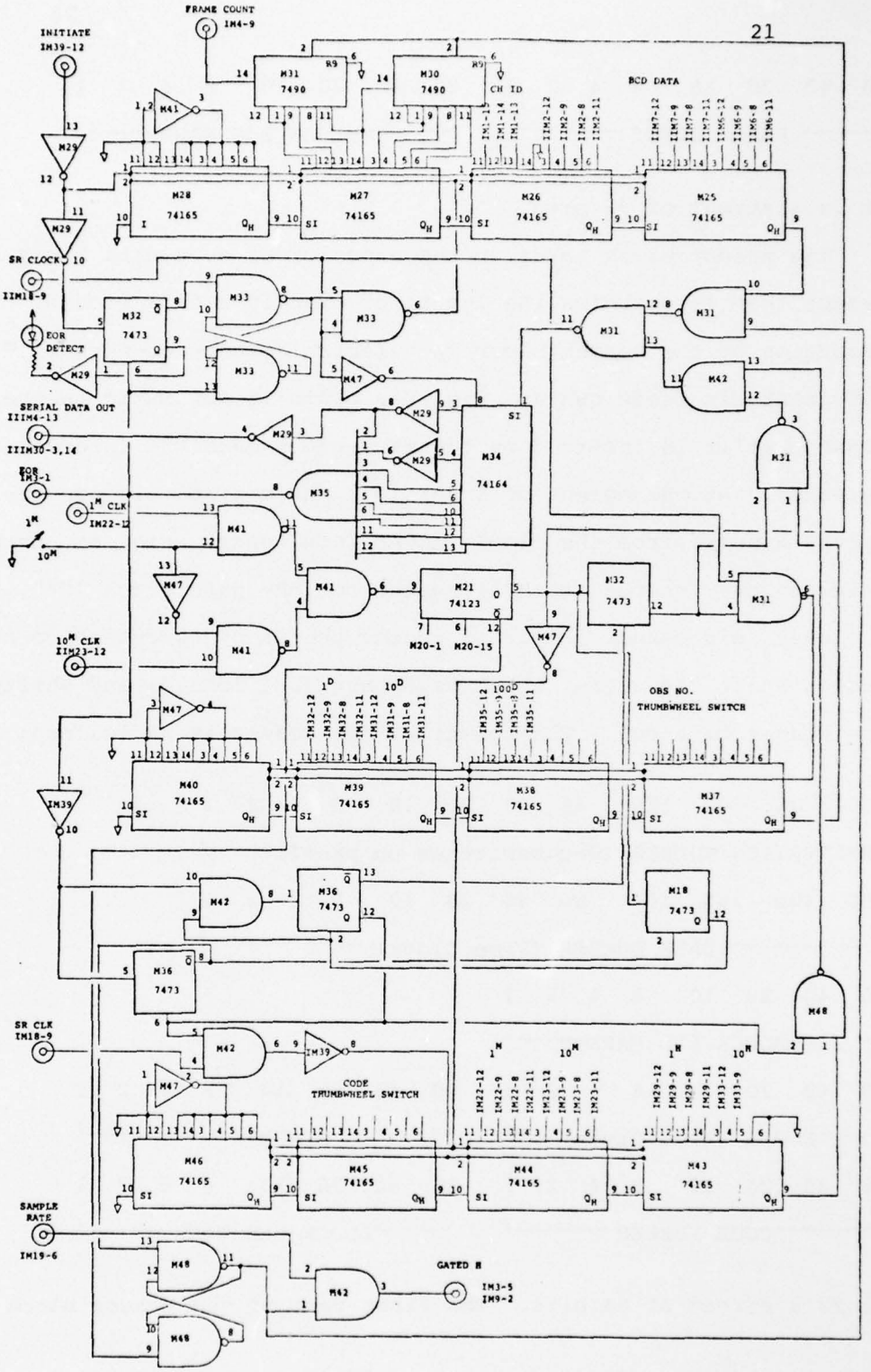


Fig. 6. Schematic diagram of Serial Data Generator and Format Control

```
80  40  20  10   8  4  2  1   80  40  20  10   8  4  2  1
└──── FRAME COUNT ──────┘     └──── BLOCK END MARK ──────┘
```

It is a stream of 32 bits.

The header block takes on the same format as a data block except that it occupies the length of exactly 2 data blocks. The insertion of the header block is selectable to be at either 1^m or 10^m intervals (left center, Fig. 6). This is automatic in the sense that it is inserted by the time clock once the interval is selected. At the moment of insertion, the control circuit receives a pulse from the clock (lower left corner, Fig. 6) through gates on M41; shapes it (M21); gates out the data block (M48, gated H, lower left corner, Fig. 6); routes the SR clock pulses to the header shift registers, which have been just loaded; and shifts the header bits out. The format of the header is as follows:

```
800  400  200  100   80  40  20  10   8  4  2  1
└OBSERVATION NUMBER (Thumbswitches on panel)──┘
800  400  200  100   80  40  20  10   8  4  2  1
└──────────DATE NUMBER (Time Clock)──────────┘
80  40  20  10   8  4  2  1
└──────BLOCK END MARK──────┘
80  40  20  10   8  4  2  1   80  40  20  10   8  4  2  1
└──── HOURS (Time Clock) ──┘   └──────── MINUTES ────────┘
80  40  20  10   8  4  2  1   80  40  20  10   8  4  2  1
└──────CODE NUMBER──────┘     └──BLOCK END MARK──────┘
```

It is a stream of 64 bits. The first part of the header block is

formed by shift registers M37, 38, 39 and 40 which are identical with those of the data block. The second part is formed by M43, 44, 45 and 46. FF's on M32, 18 and 36 with gates M31-4,5,6, M42-8,9,10 and M48-1,2,3 keep track of sequence of the bits and clocking pulses so that the first part will be followed by the second part in shifting out the bit stream.

VII. Analog to Digital Converter

Located on board IV, the A/D converter converts a 0 to +10 v analog input voltage to a 12-bit full scale binary number. The converter, ADC-12QZ, is of the successive approximation type which requires a minimum of 40μs per conversion. A buffer amplifier at its output is there to provide a high input impedance to the output of the 8 channel analog multiplexer (AM3705D). Its address is generated by the channel control circuit presented earlier in this report. Fig. 7 shows the schematic.

For convenience of readout, the output of data is in BCD form. However, the A/D converter on hand generates 12 bits of a binary number. Therefore, we describe here a conversion technique. The circuit is shown in Fig. 8, and located on board II.

For a 3-digit decimal number, the resolution is 10^{-3} which requires only 10 binary bits. Since there are 12 binary bits available, the LSB is bypassed to improve on noise fluctuations. The remaining 11 bits are then used for the conversion. The technique is first to load the 11 bits into a presettable up/down binary counter (M1, M2, M3, SN74193), then it is made to count down at 1 MHz rate. In the meantime, a set of BCD counters (M6, M7, M8, SN7490) is reset to zero and made to count up with the count down pulses for the binary counters. Those pulses are turned off (M4) when the contents of the binary counters are exhausted. When this happens, an EOC (Ready, M4-3) signal is generated signifying that the contents of the BCD counters is now equal to that of the original binary number. It is noted that 3 digit decimals only require 10 binary bits and here 11 bits are used. The

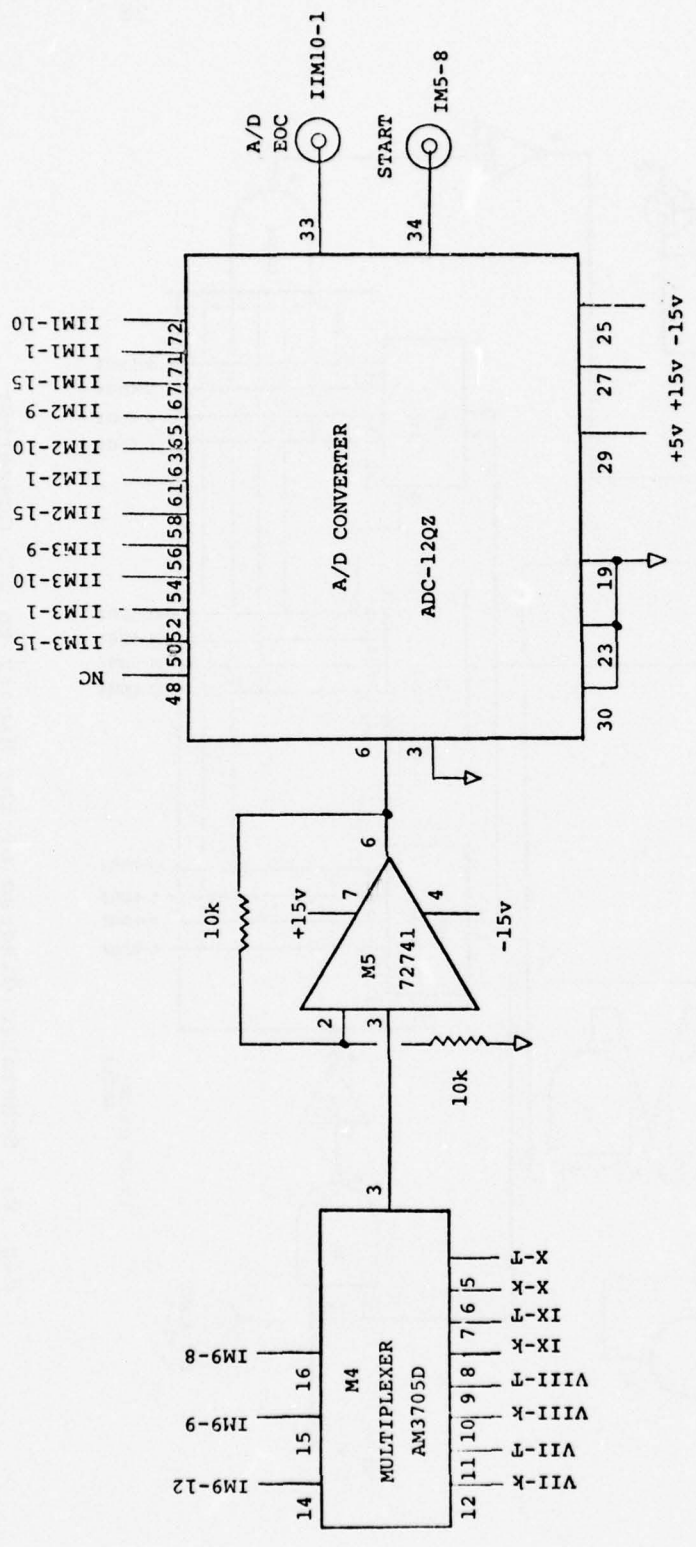


Fig. 7. Schematic diagram of Analog Multiplexer and Analog to Digital Converter

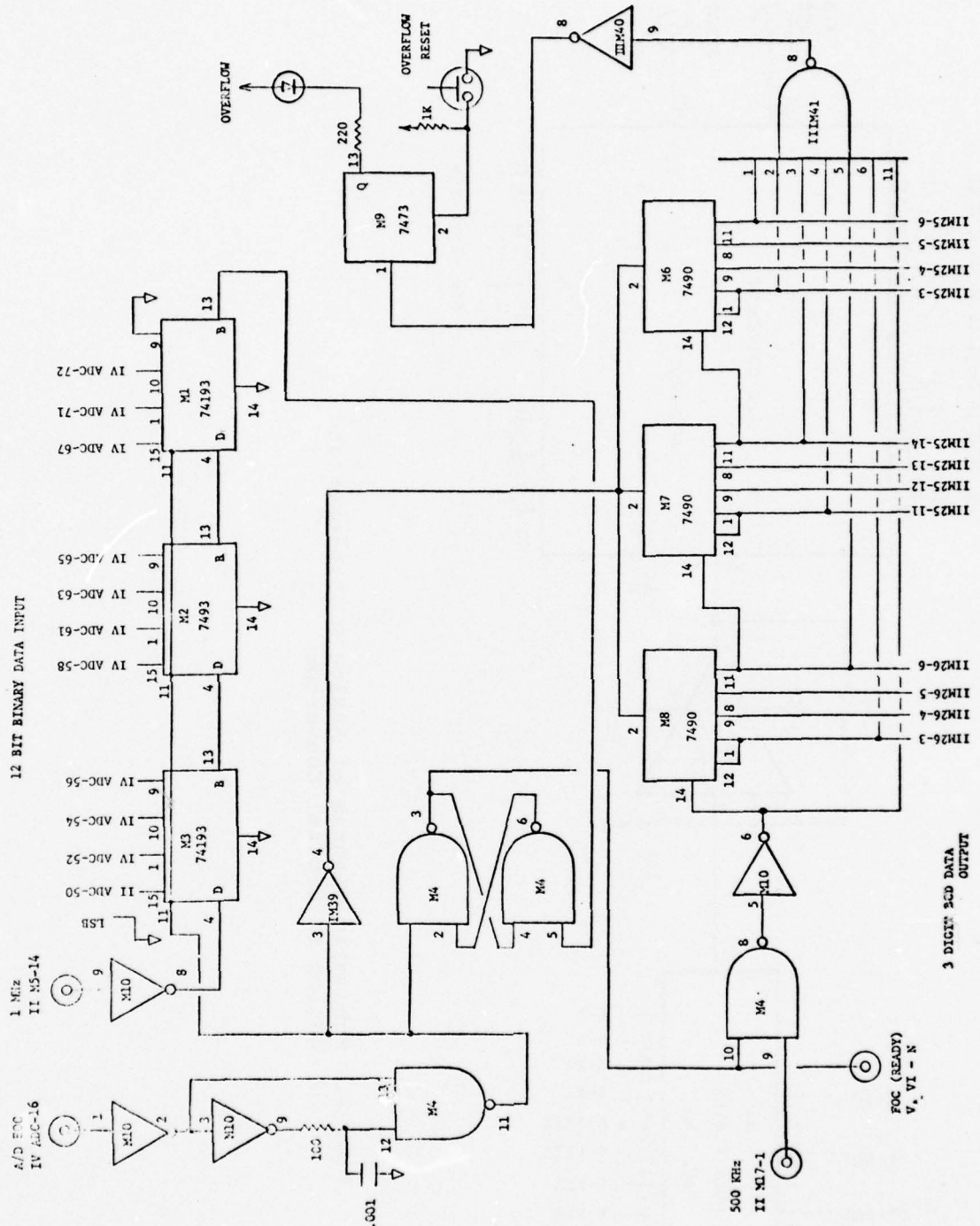


Fig. 8. Schematic diagram of the Binary to BCD Converter

discrepancy is accounted for by halving the clock rate to the BCD counters. An over-flow indicator is included (M9). A manual reset button requires the attention of the operator so that the over-flow situation can be remedied.

Another note: when it is over-flowed, the decoded data display on the control panel would read 024. It is actually reading 1024 representing the full count of a 10-bit binary number. Maximum conversion time is 2 ms for a full scale of $\pm$ 10 v. Correspondingly less time will be needed for smaller voltages.

The BCD data are presented to the formatter to be shifted out as a part of the data block bit stream.

VIII. Data Display

The operator selects the channel output to be displayed. The control, as shown in Fig. 9 and located on board III, generates the display accordingly. It should be noted that the information for the display is extracted not directly from the A/D converter but rather from the serial data stream. This is to guarantee that an error-free data stream has been generated. The serial data are first shifted into a 32-bit SR formed by M9,15,10 and 16 (SN74164). Latches (M11, M17, M23, SN7475) are used to capture the desired data to be displayed. Coincidence of channel ID number from the data stream and that selected on the selector switch is used to generate the latch command upon detection of the data block end mark (M8). M14 (SN7442) decodes the channel number which compares with the setting on selector switch through gates on M3, M1 and M2. When they compare, one-shot (M19) produces a pulse to freeze the data digits for the particular analog channel output. The digits are then encoded by the 7-segment encoder/drivers (M6, M12, M18, SN7447) for readout on the control panel. A one-shot (M21) lengthens the ID detection to about 0.5 sec and drives an LED indicator on the control panel so that it will be visible by the operator to show that a complete data block has been captured. The input gates (M4, M5) select the data stream either directly from the Serial Data Generator (pre-recording data) or from decoded data stream received through the play-back provision of the tape recorder (post-recording data). In this way, by flipping a switch on the control panel, the operator can view both data streams to see if the recording system has been operating properly.

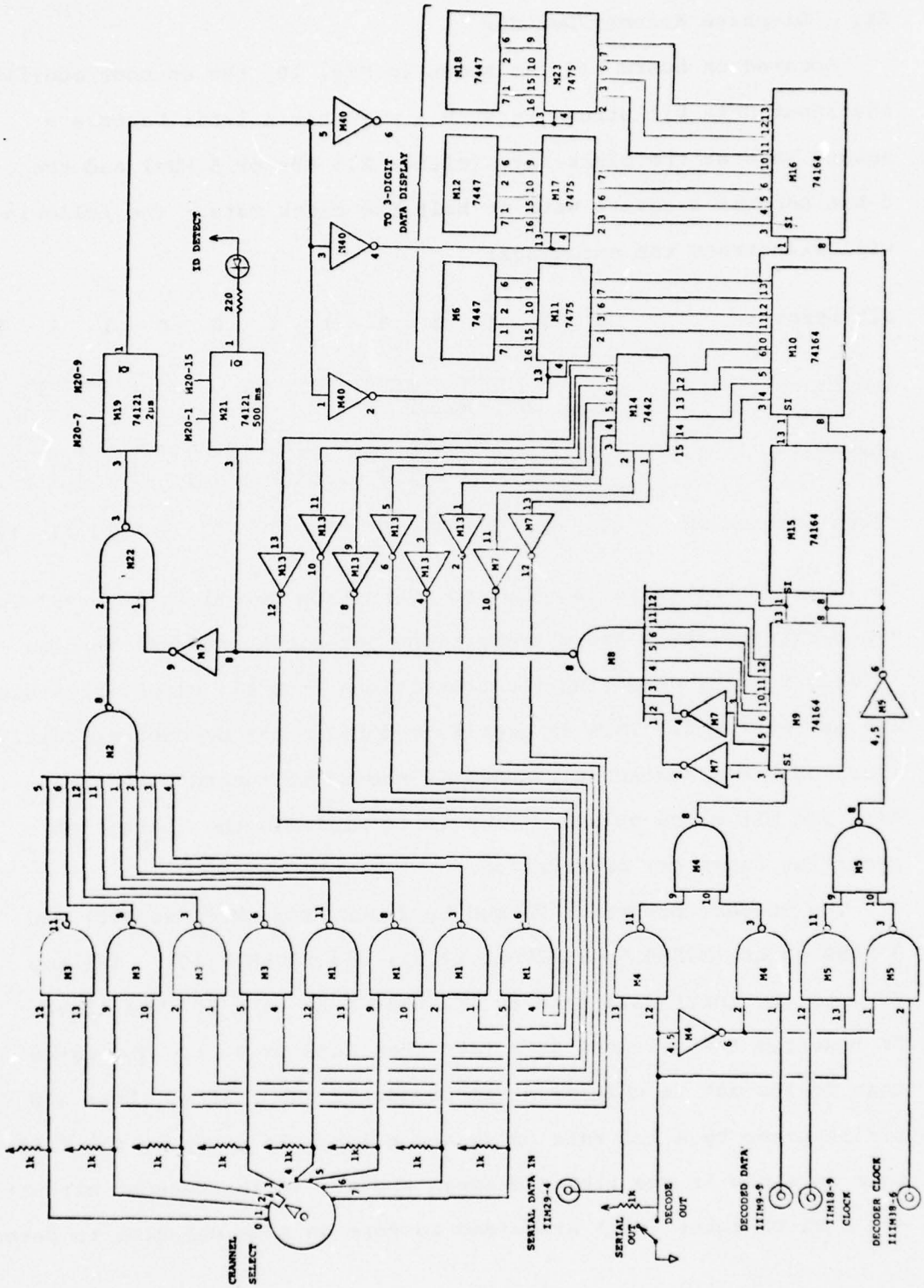
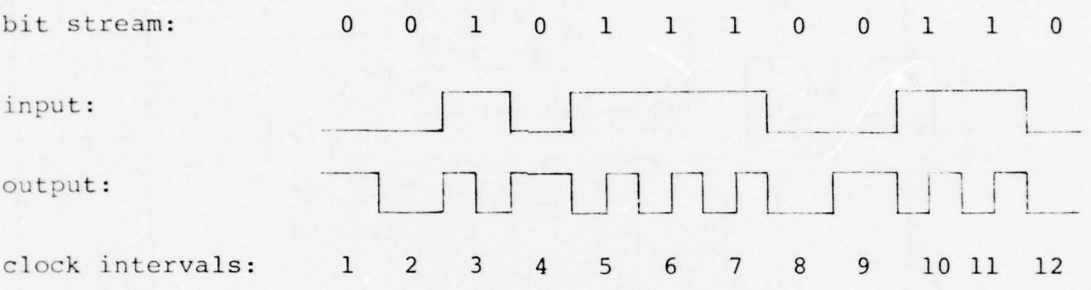


Fig. 9. Schematic diagram of Data Display

IX. Di-phase Encoder/Decoder

Located on board III, as shown in Fig. 10, the encoder modifies the input data bit stream in such a way that a 1-bit becomes a square wave at the clock rate (either 2.5 KHz or 5 KHz) and the 0-bit becomes a square wave at half the clock rate. The following will illustrate the encodings:



It is seen that there is only one transition per clock interval for the 0-bit and there are 2 transitions per clock interval for the 1-bit. Thus by detecting the transitions, the bit clock intervals can be retrieved. This is precisely done in the decoder circuit. Thus, only one recording channel is needed to record both data bits and bit clock pulses. This is to minimize the footage of recording tapes per observation.

The encoder proper is formed by 2 J-K FF's (M30, SN7473) and 3 NAND gates (M29-4,5,6; M29-11,12,13; and M29-8,9,10). The top FF cuts the input data rate by 1/2 when data is a Ø. The lower FF restores the original data rate when data is a 1. The gates that follow act to multiplex the states of the 2 FF's. Thus a Ø bit is given by a 1/2 rate pulse and a 1-bit is given by the full rate as shown in the timing diagram above. In the decoder circuit, the 4 EX-OR gates (M31) are wired to form an edge detector to detect

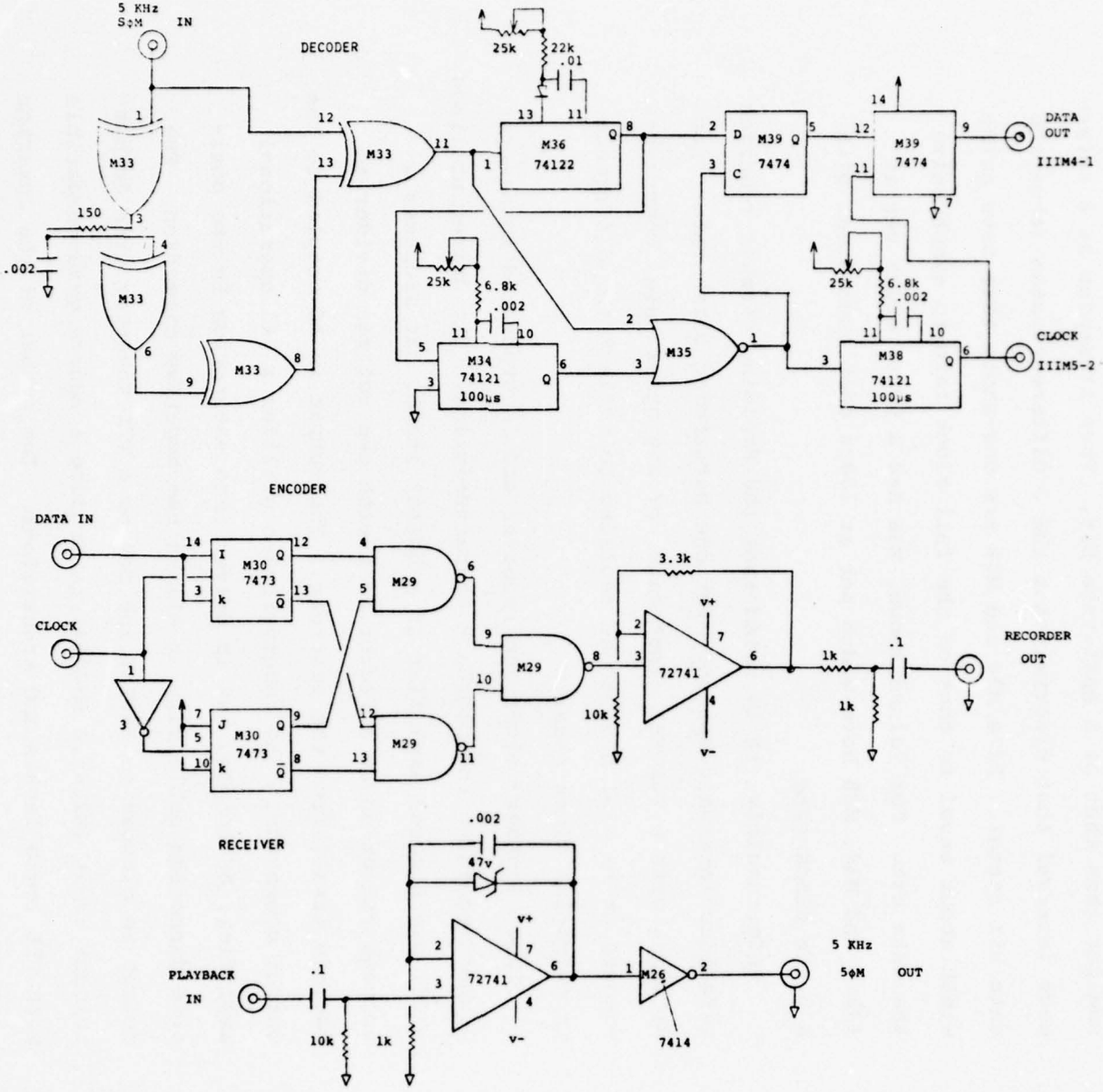


Fig. 10. Schematic diagram Di-phase Encoder/Decoder with tape recorder driver and receiver.

the high-low or low-high transitions. M36 is a one-shot with pulsewidth greater than the pulse width of a full data rate but smaller than that of a half-rate bit. Thus it serves as a reference interval that discriminates the 2 different rates (thus the data bit state). FF's M34 and M38 are one-shots that have pulse width about equal to that of the full clock rate to synchronize the data bit. For values shown, M36 has a pulse width set at 130μs and M34, M38 have width set at 100μs each consistent with a 5 KHz clock rate.

Unfortunately, it is noted that the decoding circuit requires reference intervals set only for one particular clock rate. For decoding with a 2.5 KHz clock rate, or any other rate, components mounted on M4 will have to be replaced to reflect the difference in operating clock rates.

Tape recorder driver and receiver are incorporated to assure proper recording and playback characteristics. The driver utilizes a 741 operational amplifier as a buffer stage. It produces a voltage reduction by a factor of 6 with the voltage divider to isolate itself from the recorder. The output is AC coupled to the output connector. The receiver also utilizes a 741 operational amplifier, AC coupled and is driven into saturation in the positive direction but hardly at all in the negative direction. The output is clamped to +4.7 V and fed to a TTL inverter with Schmit-trigger input (M26-1,2 SN7414) to produce a square wave compatible with TTL logic levels and transitions. The output of the inverter goes directly into the decoder input. It should be noted that the polarity inversion from this inverter is of no importance since the decoder only looks for transition rates but not the actual logic levels.

X. Analog Channels

The analog channels, on boards VII, VIII, IX, and X, prepare the analog voltage inputs for eventual digitization. Four channels are specifically designed to accept the AGC voltage output of the Model B receiver (Magnavox Company). The other channels are designed differently for accepting voltages varying between +1 to +5 VDC. However, pin assignments on all these boards are chosen such that interchangeability is preserved. For the sake of description, let's designate channels 0 through 3 to be the ones for Model B receiver, which delivers voltage ranging from -200 to -800 mv. Channels 4 through 7 are of the other kind. There are 2 identical channels built on each board.

Board VII, shown in Fig. 11, contains channels 0 and 1. The first stage operational amplifier presents a high input impedance to the incoming voltage and offsets the output by 200 mv such that the output will vary from close to 0 volts. The output is trimmable to compensate for gain variations for different receivers. A test point is also available here. It also serves to have this first stage output displayed on the panel meter so the operator may set the operating level of the Model B receiver. A unit gain buffer stage follows to isolate the input circuit from the integrator. The integrator is of the true integrating type. The feed back capacitor (.01μf) of the FET input operational amplifier is allowed to charge (or discharge) due to the input voltage through the input 100 K ohm resistor. At the end of the selected sampling period, the input FET switch is turned off such that the output of the integrator will no longer change (sample-hold action). After a

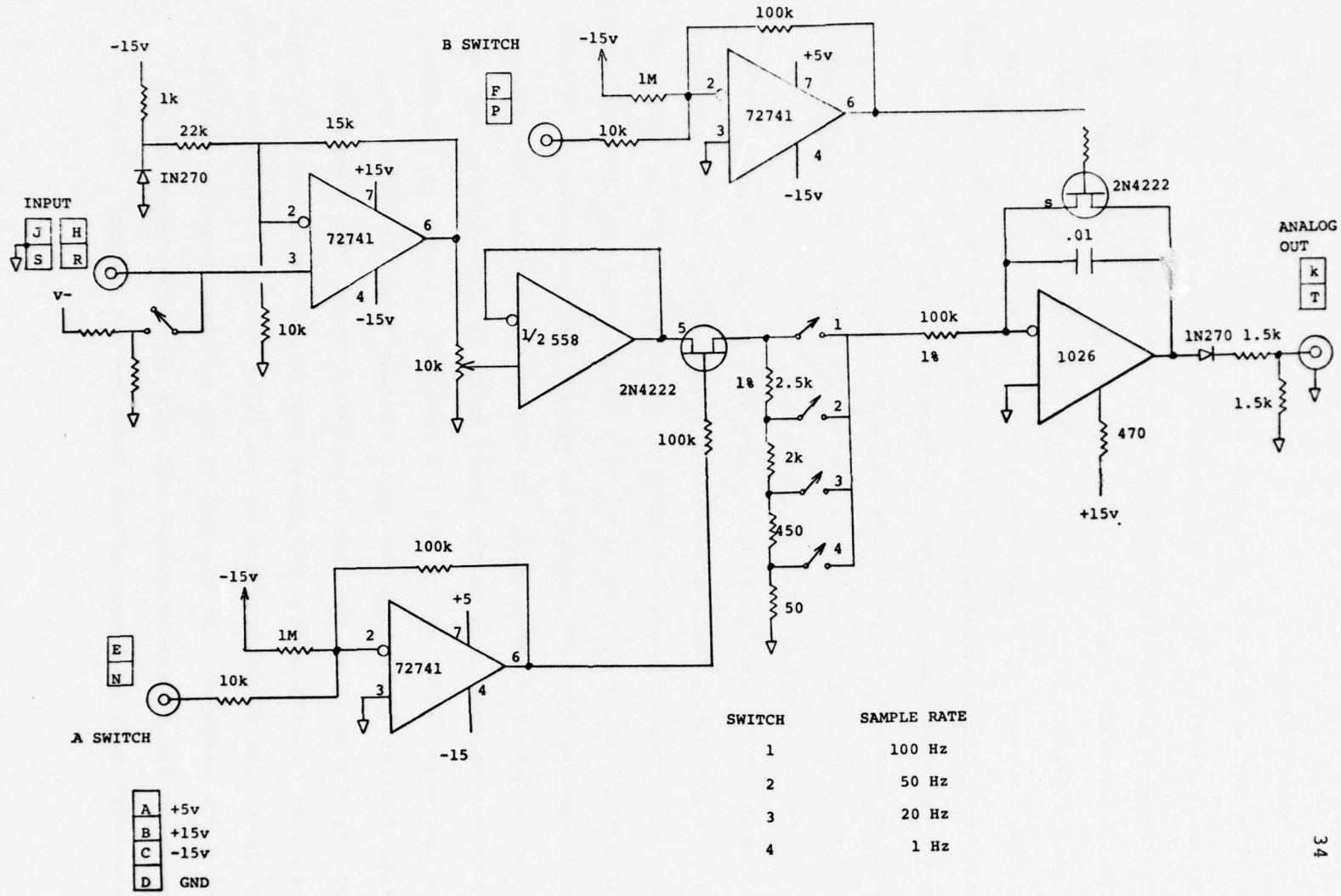


Fig. 11. Schematic diagram of low level integrating Analog Channels.

slight delay (20μs) to allow the input switch to completely turnoff, the output is channeled to the A/D converter to be digitized. At the end of conversion, the capacitor is allowed to discharge through another FET switch which turns off briefly (40μs) and in the meantime the input FET switch turns back on to begin another integrating period. In this fashion, the integrating period is the entire sampling period minus 60μs.

The voltage divider at the input of the integrator is necessary to account for the different sampling periods available for the system. The output of the integrator of this type is a direct function of the integration period. For a constant input voltage, the output will be greater if the integrating period is longer since the capacitor is allowed to charge longer. In order to make the output more or less the same for the vastly different sampling periods available, the input voltage is modified by selecting corresponding taps on the input divider circuit.

Two additional operational amplifiers are used as drivers for the two FET switches. They are directly driven with TTL logic levels generated from digital circuits.

Fig. 12 shows schematic for the other analog channels. Again, each board contains 2 identical channels. The input stage buffers the input voltage and also provides the necessary offset. A test point at the output of the first stage also allows the panel meter to read the voltage. The FET switch provides the sample-hold action. The output stage, which uses the same type of operational amplifier as the integrator, is not an integrator but a simple buffer. Therefore, the output is an instantaneous sample of the

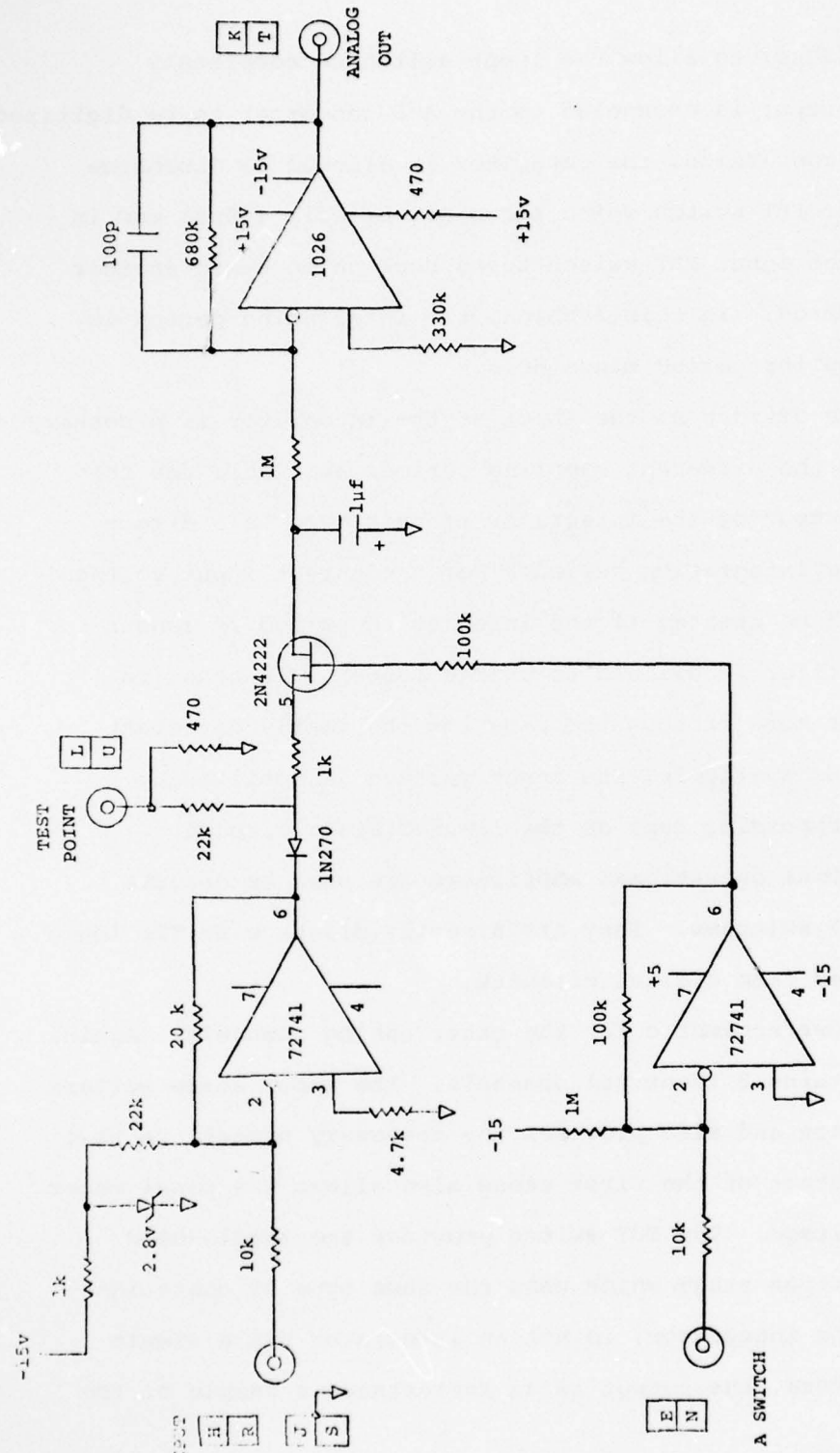


Fig. 12. Schematic diagram of sample hold Analog Channel

input voltage. Inclusion of the FET-input operational amplifier as the output stage is to facilitate modification of the channels to an integrating type at a later time if so desired.

With or without integration, the control is identical to all channels, thus making it possible to interchange placement of the channels. However, it should be noted that digital control is applied only to one channel at a time and in a sequential manner. The analog control will be described in the next section.

XI. Analog Control

Located on board V and VI, as shown in Fig. 13, the analog control starts with the reception of a sample-start pulse. Recall that each analog channel is associated with 2 FET switches. One A(N), N denoting channel number, is the sample-hold switch at the input of the integrator. The other, B(N), is the discharge switch for the integrating capacitor. One should not be distressed to note that some of the channels do not have integrators. The presence of an integrator is not necessary for the control scheme to work. In any case, the control described below sets the timing for turning on or off those switches. It also signals the digital system when to advance the channel address, when to start A/D conversion, and when to shift data out.

First of all, on receiving the sample-start pulse, (upper left corner, Fig. 13) it turns off A(0) through the J-K FF (1/2 M14). After a delay of 20μs provided by 1/2 M7 one-shot to allow enough time for the switch to be fully off, S(0) signals the Channel Control (board I) to start the A/D conversion to read channel 0 (see Channel Control IM5). When the conversion is done, a 'READY' pulse actuates B(0) to discharge the integrating capacitor for 40μs (1/2 M7, SN74123). In the meantime, initiation to generate a data block (see Channel Control IM6) is given to the Serial Data Generator to shift data out. The Channel address is incremented at this time to prepare the next channel. At the end of the 40μs, a signal is given to turn A(0) on and B(0) off to start another integration. This is done through the trailing edge detector formed by gates on M4-4,5,6, M4-1,2,3 and RC delay circuit mounted on M5. A data

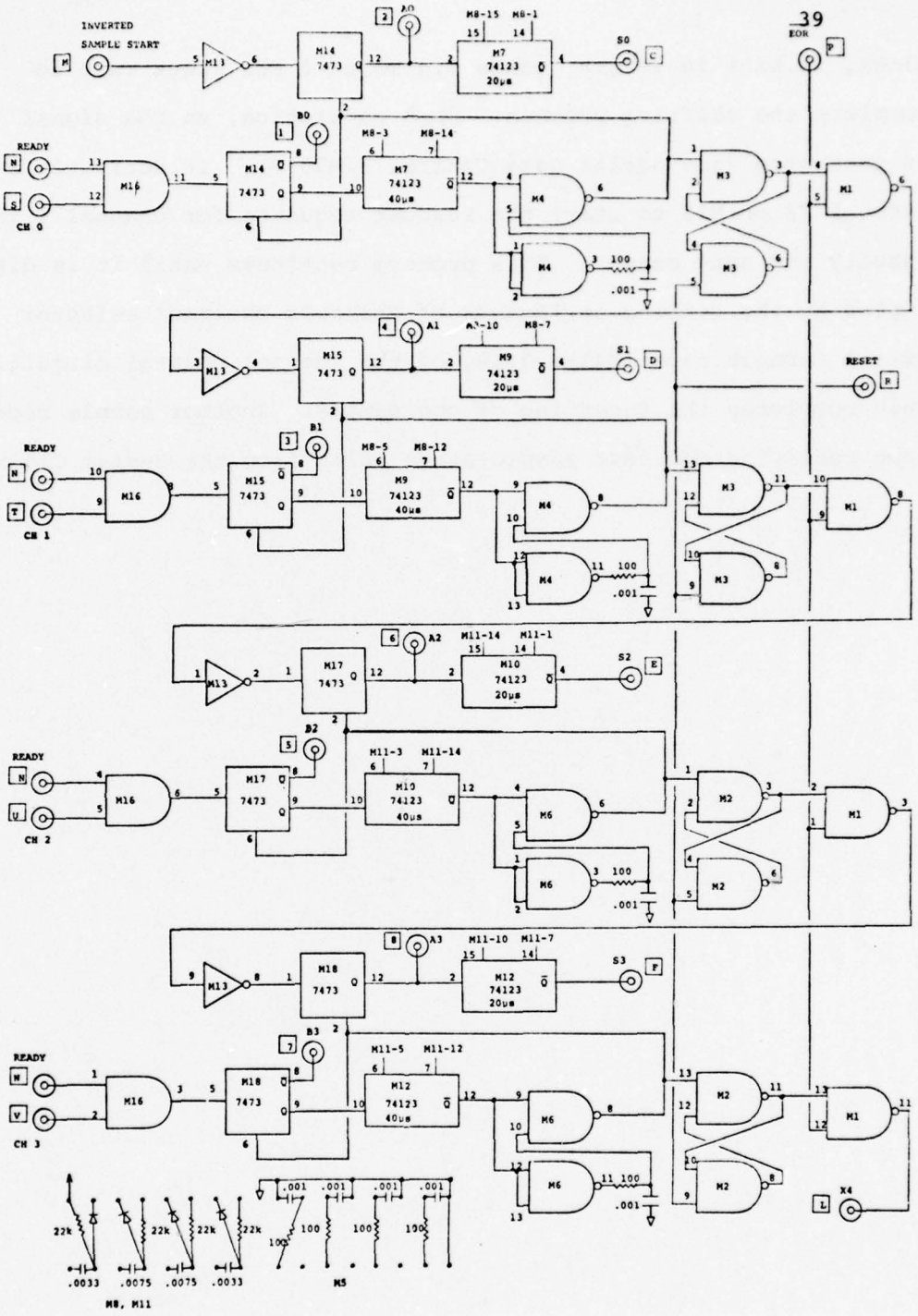


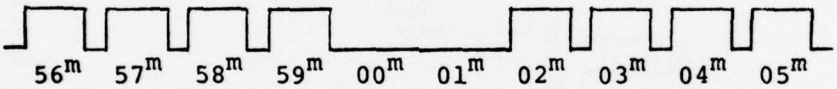
Fig. 13. Schematic diagram of Analog Control

block, 32 bits in length, takes 6.4 ms at 5 KHz clock rate to complete the shifting process. Upon completion, an EOR signal is generated (see Serial Data Control IIM35-8). It activates A(1) through FF on M15 to start the readout sequence for channel 1 in exactly the same manner. This process continues until it is disrupted by the setting on "Number of Channels Desired" selector switch through gate IM41-8,9,10, of the Channel Control circuit. This completes the recording of one sample. Another sample repeats upon receiving the next sample-start pulse from the System Clock.

XII. Shift Register Clock Rate Identifier and Time Mark Generator

Located on board III, the Shift Register Clock Rate Identifier circuit, shown in Fig. 14, produces a blinking LED indicator on the control panel to verify the clock rate by the operator. The shift clock is directly counted down by a factor of 2000. It is easily discernible as to whether the operating clock rate is 2.5 KHz or 5 KHz. Count down involves M24,25,31 and 32 (SN7490).

Also located on board III, the Time Mark Generator, shown in Fig. 15, takes in the 1^m and 1^h pulses from the time clock to produce a sequence of 1^m tick marks in the form of a relay contact closure for external use. The 1^h mark is superimposed to identify the hour mark on the same pattern. An example of the pattern is given below:



R-S FF formed by M44-8,9,10 and M44-11,12,13 does the gating. The 1^h is sensed by the trailing edge detector formed with gates M44-4,5,6, M44-1,2,3 and delay RC circuit. 2 J-K FF's (M45, SN7473) gates out exactly 2 minute-marks when the 1^h mark is sensed. The relay is a sensitive dry reed type operated directly from V_{cc} and TTL logic levels.

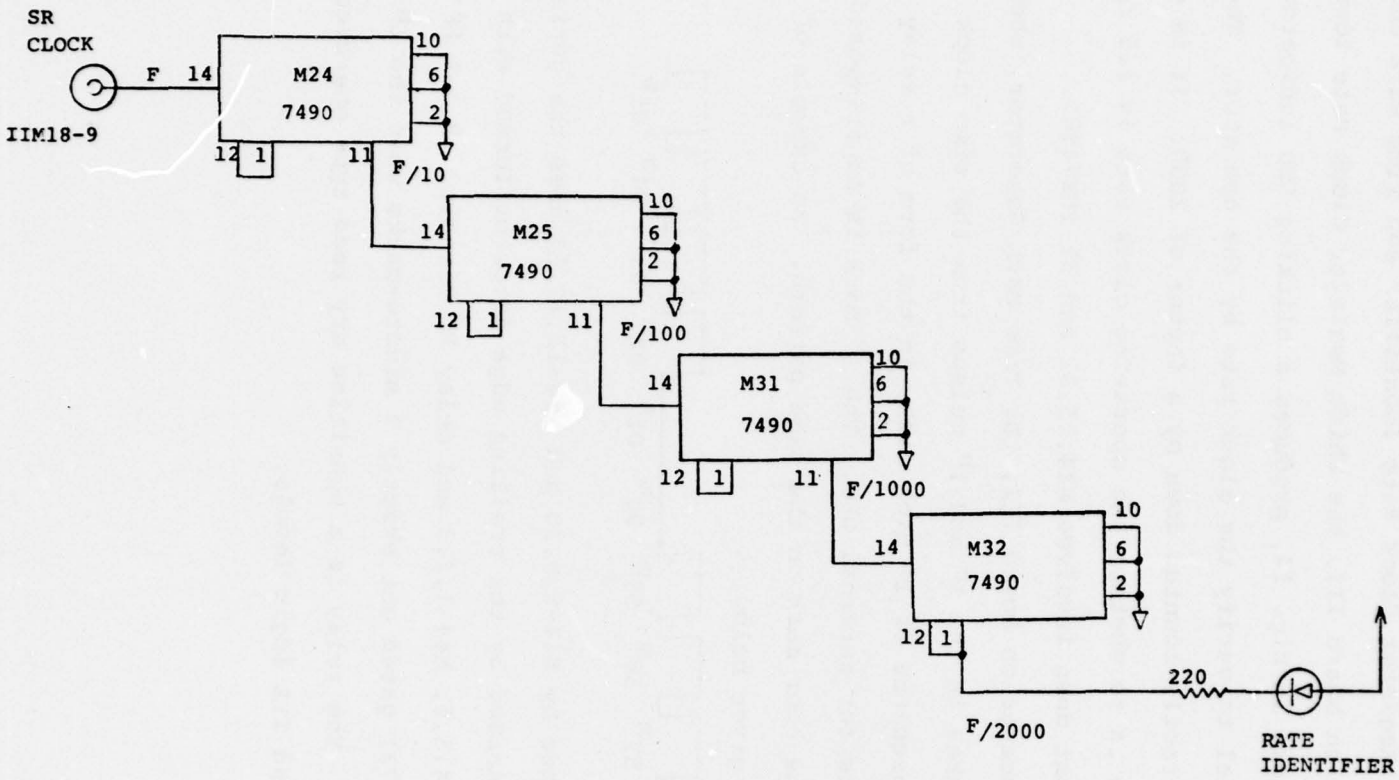


Fig. 14. Schematic diagram of Shift Register Clock Rate Identifier

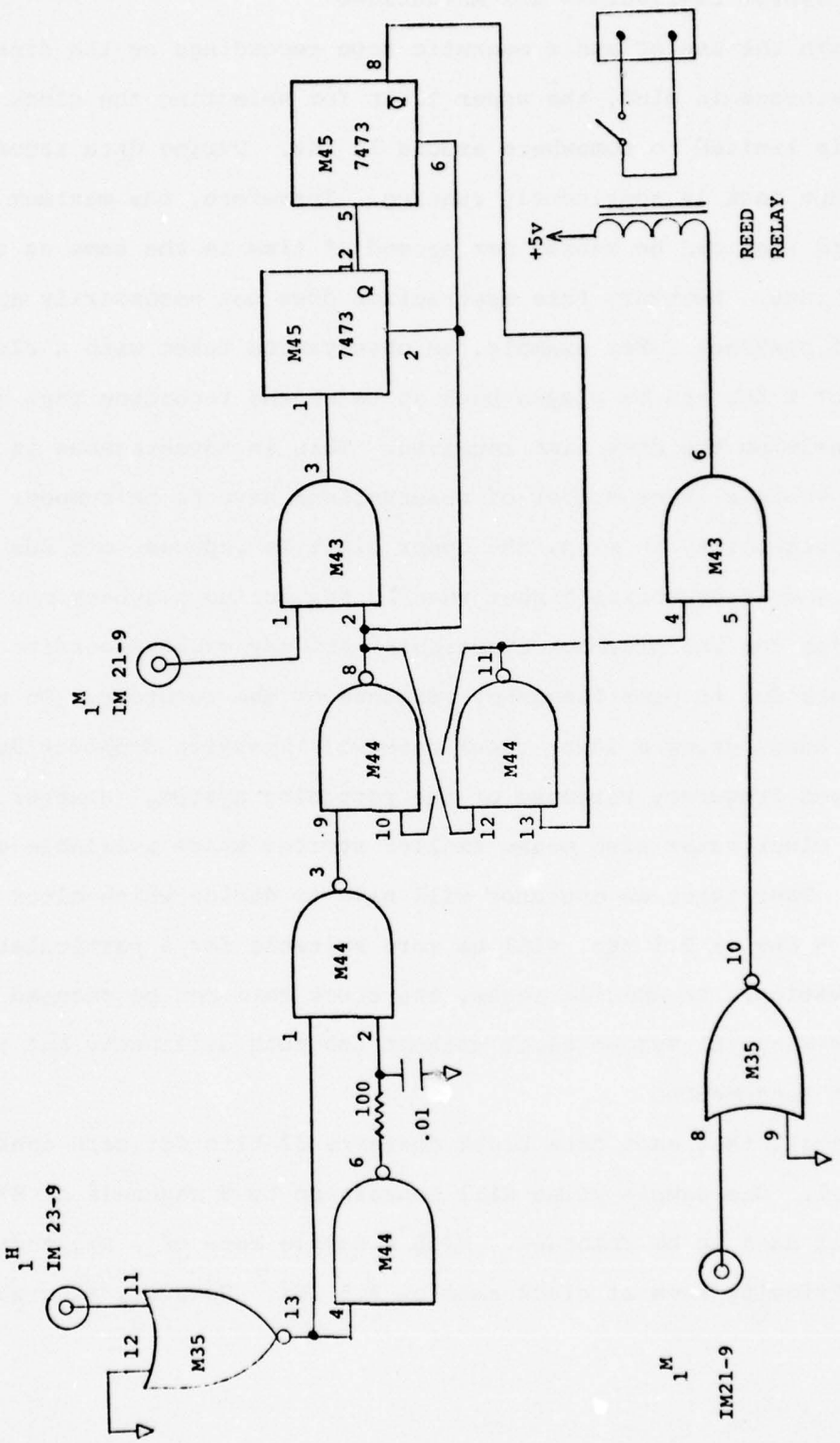


Fig. 15. Schematic diagram of Time Mark Generator

XIII. System Limitations and Advantages

With the use of audio magnetic tape recordings as the final data storage in mind, the upper limit for selecting the clock rate is limited to somewhere around 10 KHz. During data recording, the tape deck is continously running. Therefore, the maximum number of bits that can be stored per second of time is the same as the clock rate. However, this restriction does not necessarily apply during playback. For example, an observation taken with a clock rate of 5 KHz can be played back at twice the recording tape speed, thus halving the dump time required. This is advantageous in cases where a large number of observations have to be dumped. With this possibility in mind, the upper limit is reduced to 5 KHz clock rate since frequencies higher than 10 KHz during playback may be too high for the playback electronics and may cause excessive dropouts due to poor frequency response of the recorder. On the other hand, using a lower clock rate will minimize dropouts due to improved frequency response of the recording system. However, lower clock rates also means smaller storage space available on tape. Therefore, an operator will have to decide which clock rate, 5 KHz or 2.5 KHz, will be more suitable for a particular observation. In special cases, the clock rate can be changed by rewiring the system clock without too much difficulty but it is not recommended.

Recall that each data block contains 32 bits for each analog channel. One sample point will contain up to 8 channels or $8 \times 32 = 256$ bits of data to be recorded. With a sample rate of 1 Hz, there is no difficulty even at clock rate of 2.5 KHz. However, at a sample

rate of, say 20 Hz, each sample will have only 50 ms to record the data. At 2.5 KHz rate, each bit takes 0.4 ms and a single data block takes 12.8 ms. This implies that only 3 data blocks can be accomodated. At 5 KHz rate, each bit takes 0.2 ms and a single data block takes 6.4 ms, or 7 analog channels can be recorded without loss. The following table will show this clearly.

Sample rate	Clock rate	Maximum number of channels may be recorded
1 Hz	2.5 KHz	8
	5 KHz	8
20 Hz	2.5 KHz	3
	5 KHz	7
50 Hz	2.5 KHz	1
	5 KHz	3
100 Hz	2.5 KHz	0
	5 KHz	1

In cases where the operator makes an error in selecting the acceptable number of channels to be recorded with respect to the selected sample rate, spillover will occur. However, this is not fatal in the sense that the system will cease to operate and no valid data will be recorded at all. Data still can be retrieved successfully for those completed data blocks. However, the contents of the block or blocks that spill over to the next sample period will be lost.

Inevitably, due to imperfections on magnetic tape and electronics in the tape recorder, there will be drop-outs, that is, some data blocks will not have the required format for detection. If this happens, the data block end mark will not appear in the

proper places and therefore, that particular block will not be detected at all. However, if this happens, the complete sample which certainly will contain some good channels will not be destroyed altogether. This is due to the fact that each frame or sample is properly identified with the frame count, thus each dropout affects only one block in one sample but not the whole sample. It should be noted that the successful detection of an end mark guarantees that all bits in the block are in their proper location, therefore, it represents a valid data point.

APPENDIX A

Now we shall describe a system capable of retrieving the recorded data and transferring them to a digital tape deck. The tape deck we shall use is a Kennedy 1600/360 9 track incremental digital deck. The maximum asynchronous record speed is 500 bytes per second. Each byte can accomodate 2 4-bit BCD digits. Therefore, we can hope to transfer data at a rate of 4000 bits per second. Recall that the data bit stream clocked at 5 KHz will contain 5000 bits per second. It seems that we should impose a further restriction on the channel number/clock rate ratio. However, this is not the case. Recall again, that each data block, though containing 32 bits, contain only 24 bits of useful data. 8 of the 32 bits are end marks and they need not be transfered for data analysis. Therefore, the effective data rate, discounting the end mark bits, is 3750 bits per second, well within the capability of the Kennedy tape deck.

The design for packing data onto the Kennedy takes the above situation into consideration and also provides readouts for all pertinent data including 3-digit decimal channel output, channel number and frame count. The device will be self-contained since it is not an integral part of the system described previously. It is a stand-alone system only requiring the di-phase coded bit stream fed to it from playing back the audio data tape. A selector switch selects the channel to be displayed. Output jacks are provided to view the raw bit stream, the decoded data, and the data clock pulses. In addition, a sync pulse is provided to sync a viewing scope for the display of data stream of the selected

channel. An LED indicator will flash each time an end mark is successfully detected signifying the presence of a new valid data point.

The system block diagram is shown in Fig. A.1. Details of the blocks will be described in the following paragraphs. Fig. A.2 shows the schematic for the Receiver/Driver circuit and conversion circuit of serial data into parallel data. Fig. A.3 is the schematic for the Kennedy tape deck interface with the record gap command generator given in Fig. A.4. Fig. A.5 shows the display selection circuit and Fig. A.6 is the readout latch. Fig. A.7 is the schematic for the readout scanner.

In reading the following descriptions, the reader is urged to always refer them to the system block diagram shown in Fig. A.1, in order to understand the function of each block with respect to the whole system.

Referring to Fig. A.2, two operational amplifiers of the "Norton" type (LM3900) are wired as the receiver and pulse shaper for the signal fed by the playback of the audio tape recorder. M1-1,2 (SN7414) is an inverter with Schmit-trigger input to further sharpen the pulses. The circuit immediately following is the edge detector with the decoder logics. Both decoded data and clock pulses are buffered as test signals available at the front panel, and also they are used to shift the data into a 32-bit shift register made up by M20,21,22 and 23 (SN74164). NAND gate M14 serve as the end mark detector. At the instant of detection, the contents of the shift register are strobed into latches (M17, 18, and 19, SN74100) by a one-shot (M15). This action temporarily freezes the input data to wait for packing onto the digital tape deck. In the mean

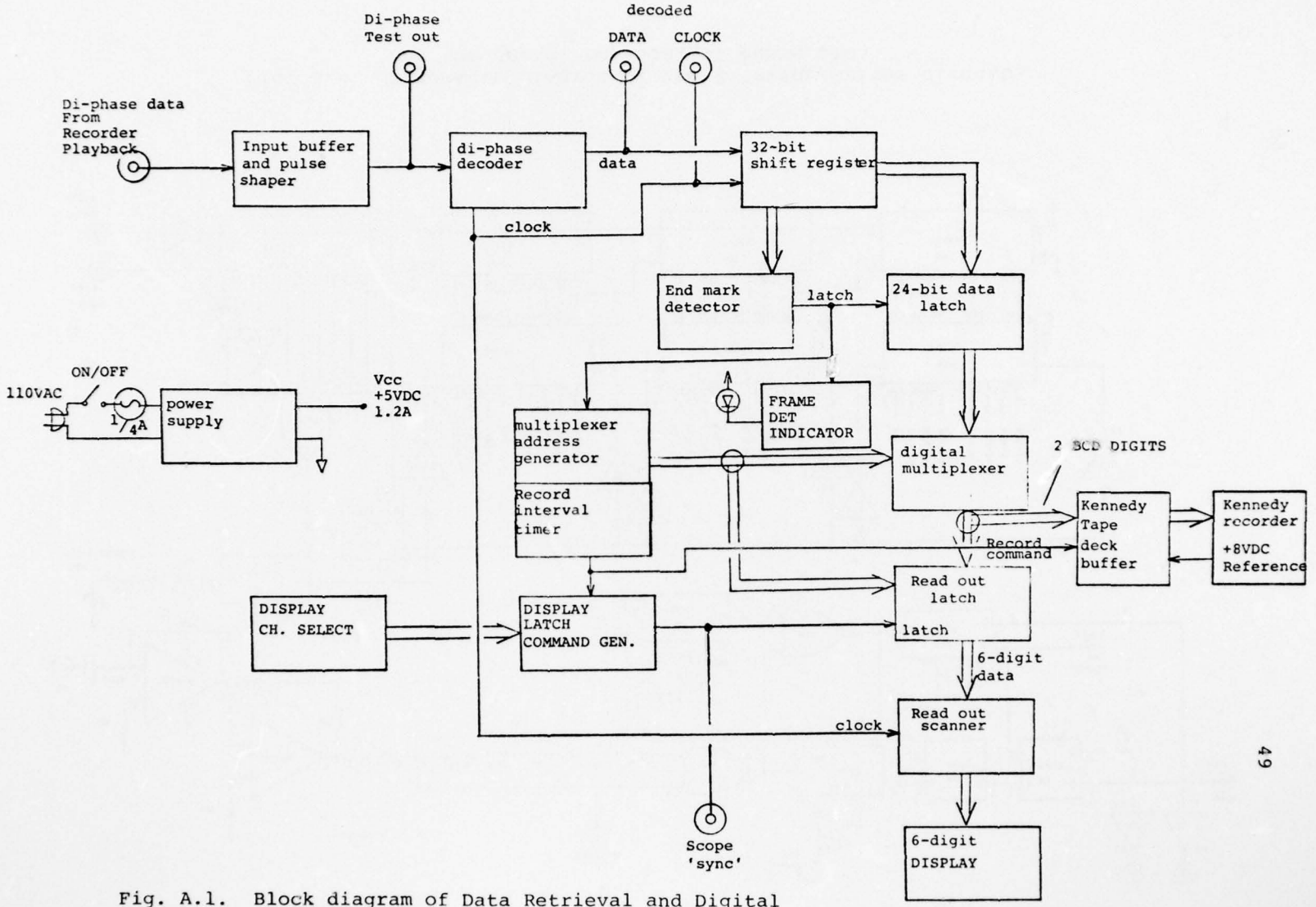


Fig. A.1. Block diagram of Data Retrieval and Digital Packing System

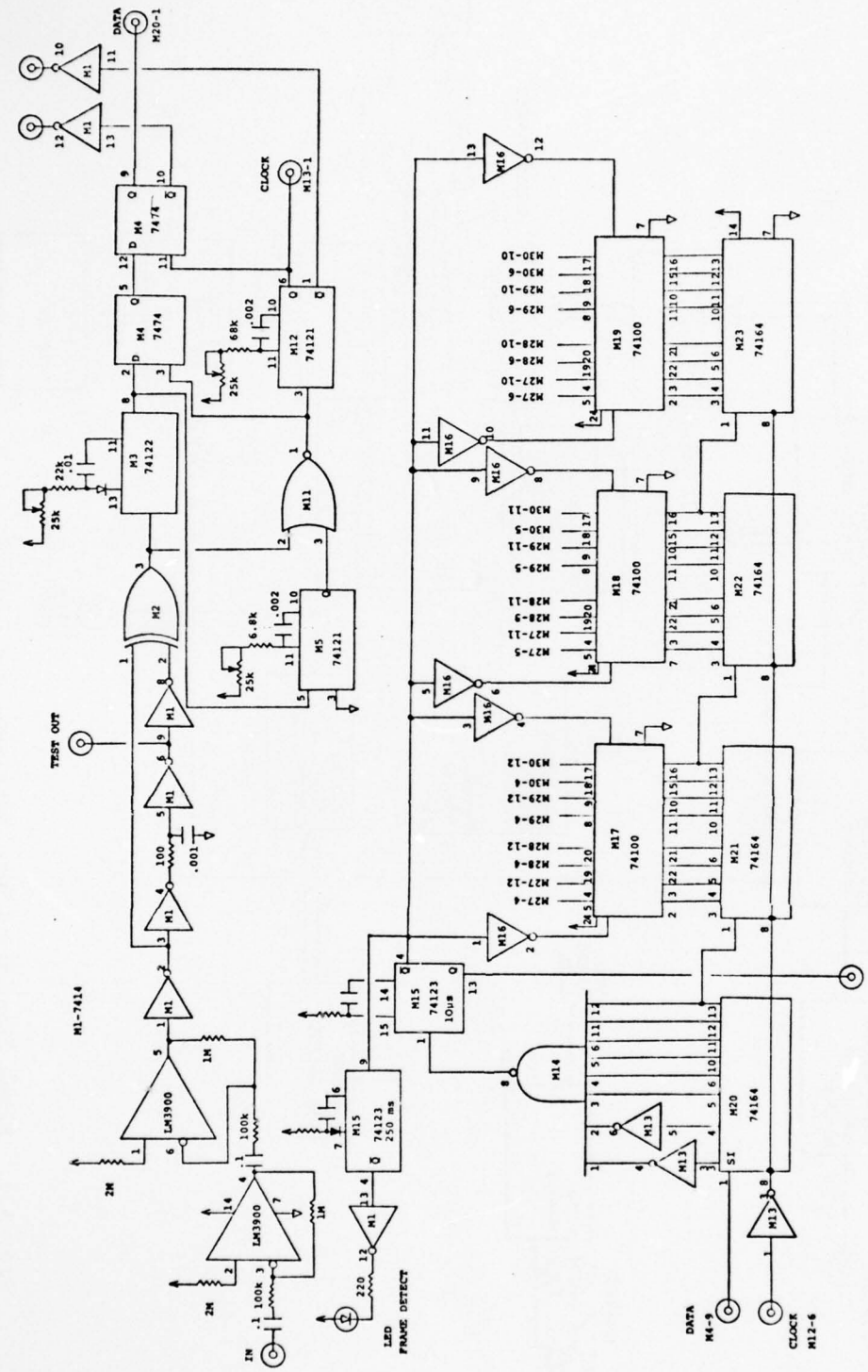


Fig. A.2. Schematic diagram of the Receiver/Driver circuit and the Serial-to-Parallel conversion

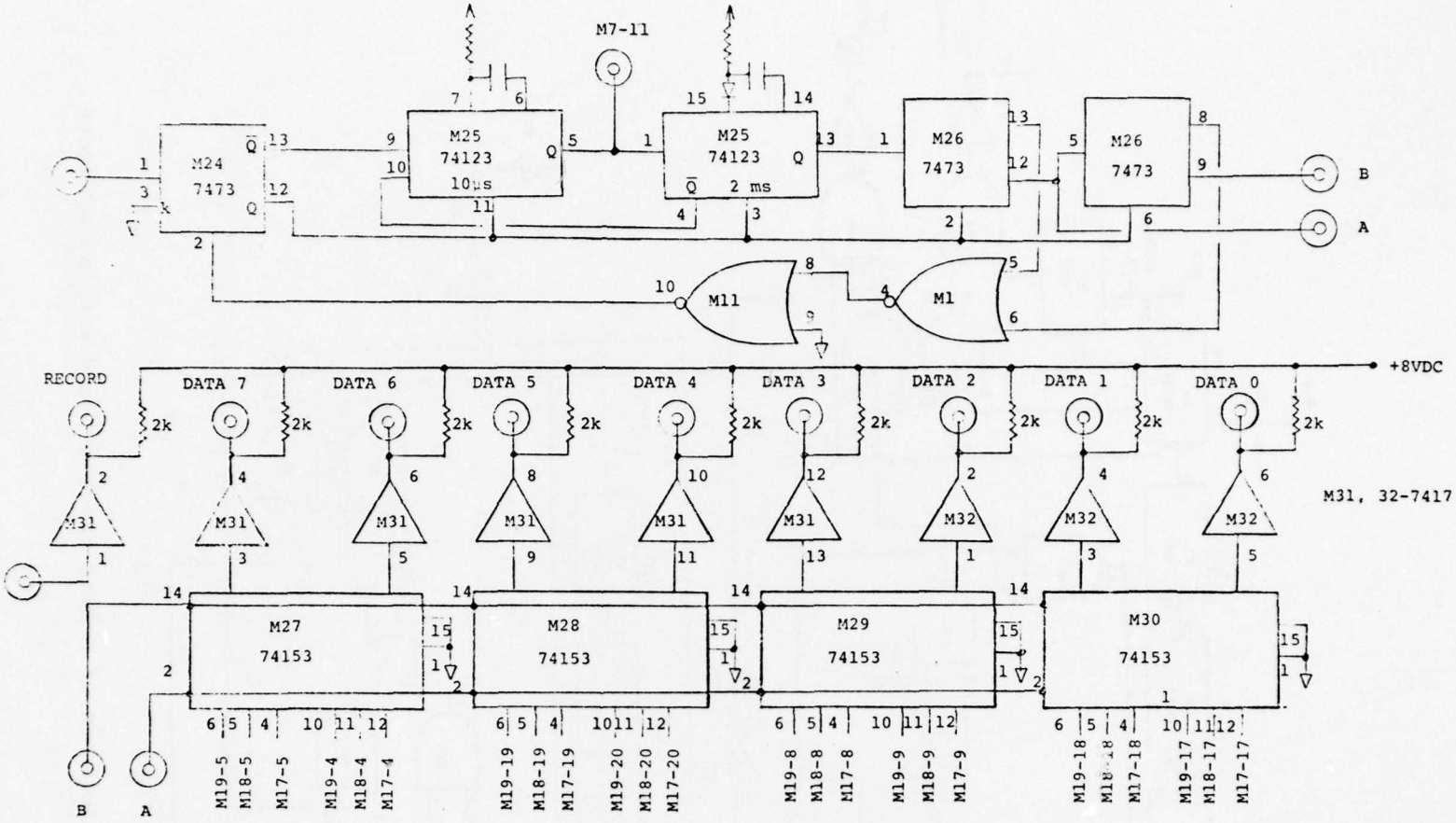


Fig. A.3. Schematic diagram of the Kennedy Tape Deck Interface

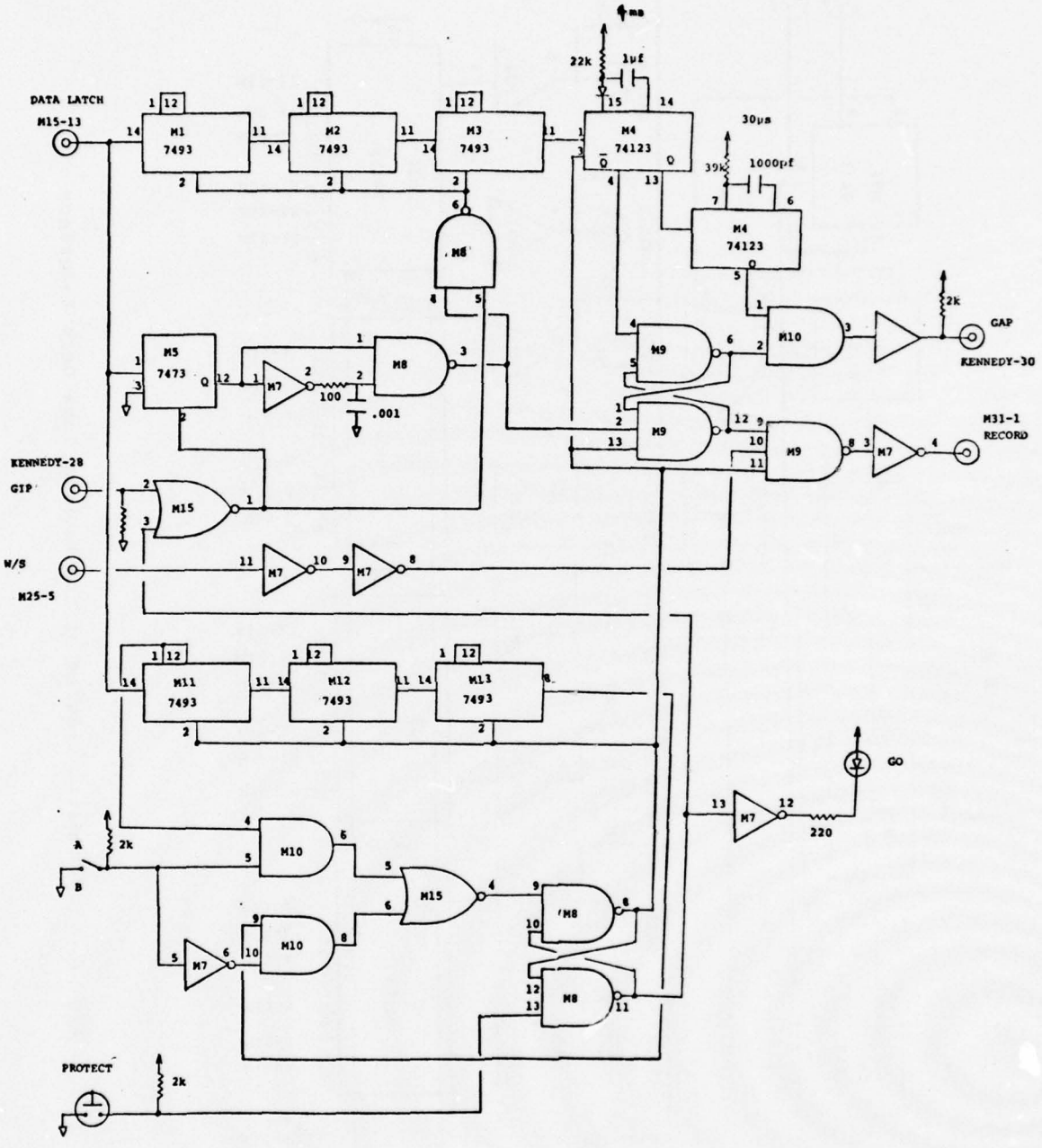


Fig. A.4. Diagram of record gap generator with delay start

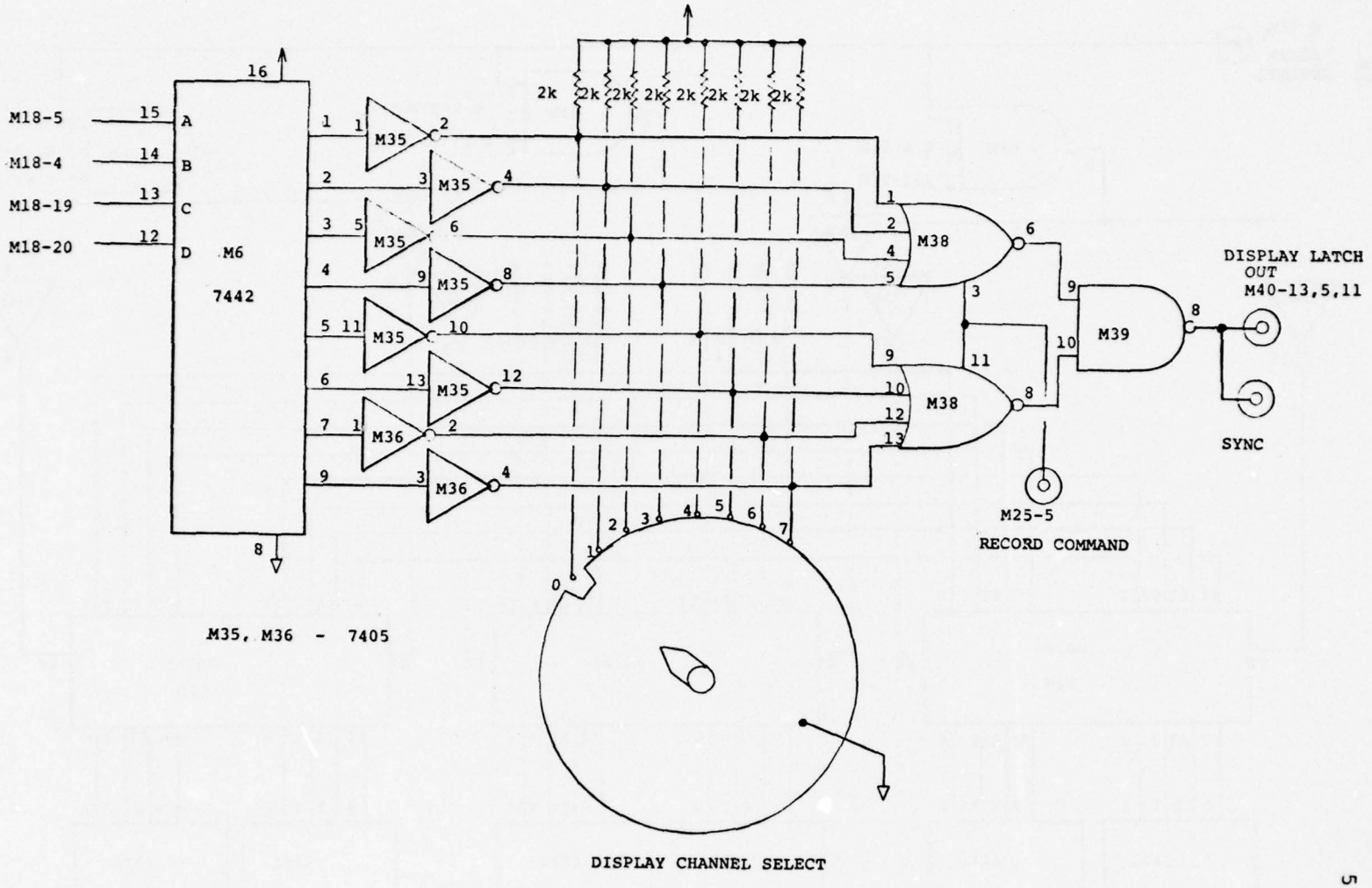


Fig. A.5. Diagram of display selector circuit.

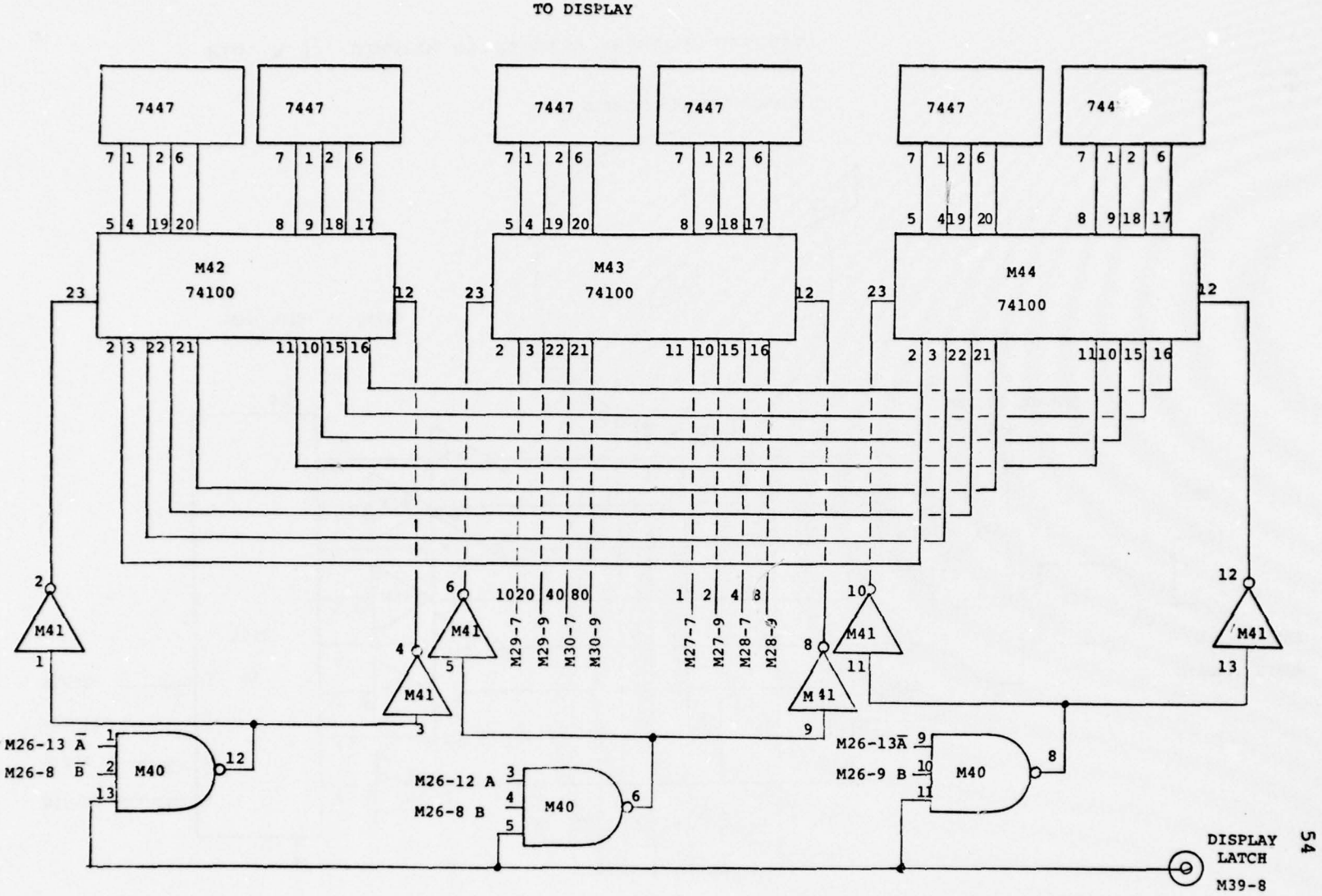


Fig. A.6. Schematic diagram of the Readout Latch

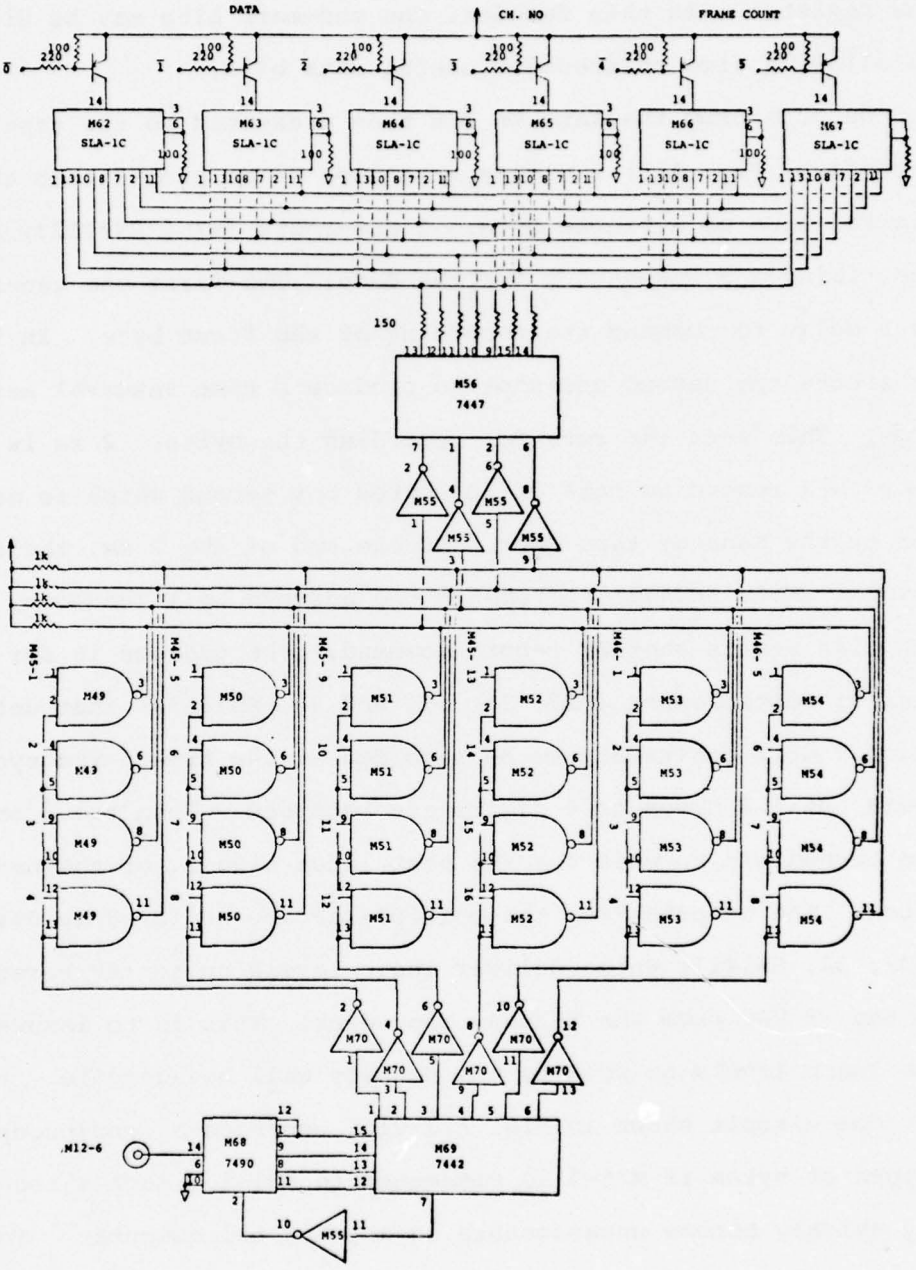


Fig. A.7. Schematic diagram of the Readout Scanner

time, the input data stream is being continuously shifted into the register. In this fashion, the end-mark bits may be discounted in allowing time to transfer useful data bits.

Outputs from the latches are then presented to the tape deck interface (Fig. A.3) 2 digits at a time to be packed onto the digital tape as a single byte. 2 one-shots (M25, SN74123) manage the timing and sequencing for the dump. The first one generates a 10μs pulse to command the recording of the first byte. In turn, it starts the second one-shot to produce a time interval set to 2 ms. This sets the rate for recording the bytes. 2 ms is equivalent to a recording rate of 500 bytes per second which is called for by the Kennedy tape deck. At the end of the 2 ms, the address counter (M26, SN7473) increments the address by 1 (coded by A, B) and also starts another record command. The address is for the digital multiplexers (M27, 28, 29, and 30, SN74153) that determine which 2 data digits are to be recorded at the time. The cycle repeats until 3 bytes or 6 digits are recorded. Then the 2 one-shots are turned off to wait for the next latch signal, or the next data block. The outputs from the multiplexer are buffered by drivers (M31, 32, SN7417) which deliver logic levels up to +8V referenced to the +8 VDC from the Kennedy tape deck. This is to insure that the logic levels as seen by the Kennedy will be adequate.

The circuit shown in Fig. A.3 will generate a continuous record of bytes if M25-5 is connected to M31-1. Such a record may quickly become unmanageable on any digital computer. To remedy this, the record gap generator with delay start shown in Fig. A.4 is inserted between these two pins. Modules M1 through

M3 provide a count to 4096 allowing 12288 bytes to be written followed by a standard record gap. Since this recording is done in real time data is lost during the record gap. To overcome this a delay start has been included with the counters M11 through M13 and chosen the switch in the lower left hand portion of the figure in position B. This allows a delay of 2048 counts (6144 bytes) before the first record is initiated. By recording once in position A and once in position B the lost data due to the record gap can be retrieved with the appropriate software.

Fig. A.5 shows how the display latch signal is generated by comparing the selector switch setting with the channel number decoded through M6 (SN7442). This scheme differs slightly from that shown in the Data Display section (see Section VIII, Fig. 9). It is more compact and efficient by using open-collector inverters (M35 and 36, SN7405) and NOR gates with strobes (M38, SN7425). It is readily seen that only when the switch setting and channel number coincide, do the NOR gates allow a signal to pass. This signal is used to latch the display. Also a 'SYNC' pulse is taken out here and may be used externally to sync a scope for viewing the data bit stream.

Fig. A.6 shows the display latches (M42, 43, and 44, SN74100). The inputs to the latches are actually taken from the outputs of the multiplexers that generate the digital byte (see Fig. A.1) to be recorded. Therefore, the display shows the actual digits just before being recorded. This is to take out the possible ambiguity that may arise due to malfunction of intervening circuits. In other words, one views the display as an exact replica of the

bytes recorded on Kennedy.

In order to conserve supply power available for this device (1.2 A @+5VDC), the readouts are scanned in time such that only 1 digit is under power at any time yet all 6 digits can be displayed. Fig. A.7 shows the schematic for the scanner and its associated 7 segment encoder/driver (M56, SN7447). The scanner, a 6-bit ring counter, is composed of a decade counter (M68, SN7490) and a decimal converter (M69, SN7442) shown in center-left of Fig. A.7. The clock for the counter is taken from the decoded clock pulses (M12-6), normally at 5 KHz. Therefore, in case of bad recordings where clock pulses cannot be retrieved, the scanner will not function, making the Display read only 1 digit instead of the normal 6. Operator's attention is thus called to the problem, and corrective measure can be instituted instead of producing a blank digital tape. More important, if data input to the system is absent, that is, if the operator failed to connect the input properly, the same phenomenon will prevail.

It is clear that the readout mechanism does not depend on the Kennedy tape deck to function. Therefore, one may wish to use it to view any particular channel output during playback as if the recording were made in real time. With the addition of an approprite digital to analog converter, one may even be able to generate a strip chart recording if so desired. Since there is no time compression scheme involved, this device can actually be used along side the data logging system in real time to dump data onto the Kennedy tape deck.

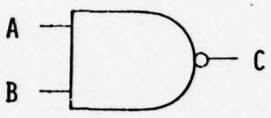
It should be noted also that the Kennedy 1600/360 tape deck we

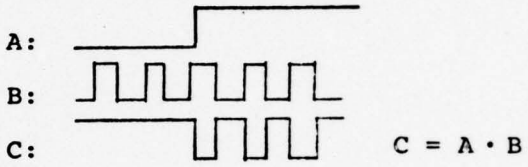
have been talking about here is of a general purpose standard type. Practically any commercial incremental tape deck has similar characteristics. The differences may lie only in data logic levels and speed. At most a bank of level shifters can make the transition possible. The speed consideration is more important. It may or may not be required to impose further restrictions on the channel number/clock rate ratio discussed in Section XIII of this report.

APPENDIX B

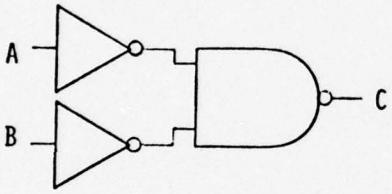
For those readers of this report not familiar with logic circuits, some explanations of so called logic "building blocks" that appeared often in this system are in order. First the "building block" circuit will be listed and then a timing or "truth" diagram will follow it to identify its function.

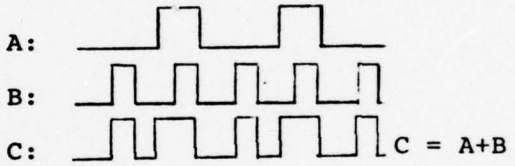
1. Basic NAND gate



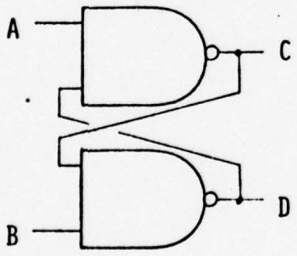


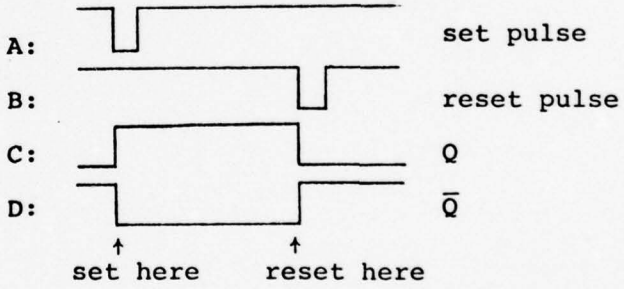
2. NAND gates used as OR



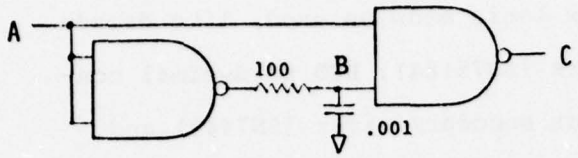


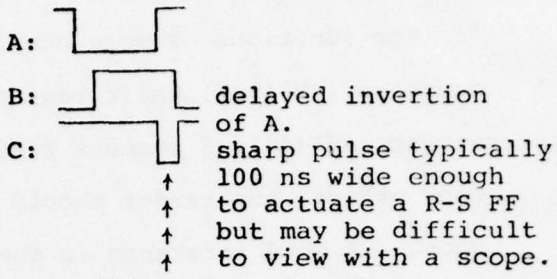
3. R-S Flip-flop (FF)



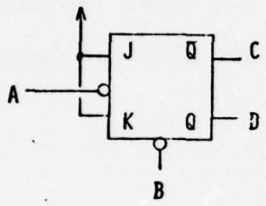


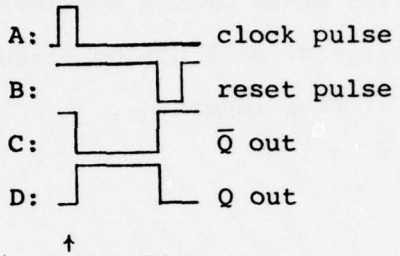
4. Trailing edge detector



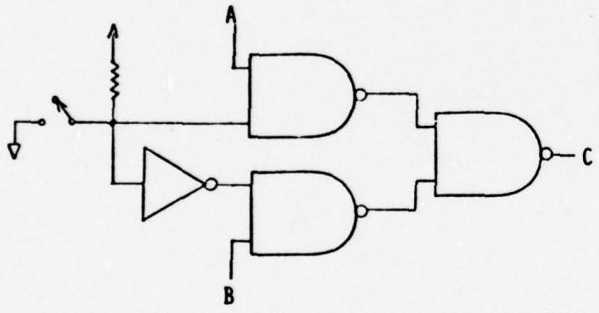


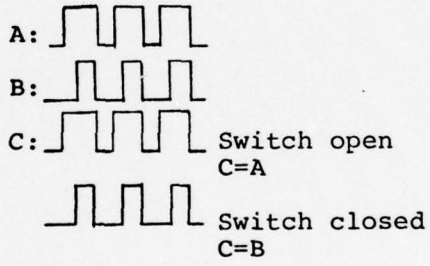
5. J-K FF (SN7473)





6. Digital switch





For functions of more complex logic modules used, like decade counters (SN7490), shift registers (SN75164), BCD to decimal converter (SN7442), 7 segment readout encoder/driver (SN7447) and many others, the reader should consult literature available elsewhere. A good reference is the TTL DATA BOOK published by Texas Instruments, Inc. They are listed according to the module's type numbers. Other design considerations, like layouts, fan-out capability, etc. will not be discussed here since they are beyond the scope of this report.

APPENDIX C

The digital tape which was produced by the equipment previously described in Appendix A is not in a form convenient for further data processing. Here we present the software necessary to unpack this digital tape, check for errors, construct a single time series from the overlapping data files, and store the data in a more convenient form. This software is divided into two stages. All programming is in Fortran with JCL for the Cyber 175 system at the University of Illinois. A complete listing appears at the end of this Appendix.

Fig. C.1 illustrates the general flow for the program UNWIND which constitutes the first stage of our software. The subroutines used with UNWIND are CONDEN, HEADER and DATCHK. Basically this stage unpacks the Kennedy produced tape and checks for errors or bad data.

More specifically, the main program UNWIND reads in the Kennedy produced tape and breaks the 60-bit Cyber word in to four bit segments with the masking operation. Each of these groups of four bits corresponds to one BCD number, and every 24 consecutive bits (or six digits) represents one of our data or header words. After these digits have been unpacked in the computer memory, subroutine CONDEN undertakes the task of reconstructing the data and header information. In the first step of this reconstruction, all of the header words are located by the subroutine HEADER. These words are located by keying on the 3-digit observation number and the 2-digit code number which are data card inputs. Subroutine CONDEN now constructs all of the data numbers while using sub-

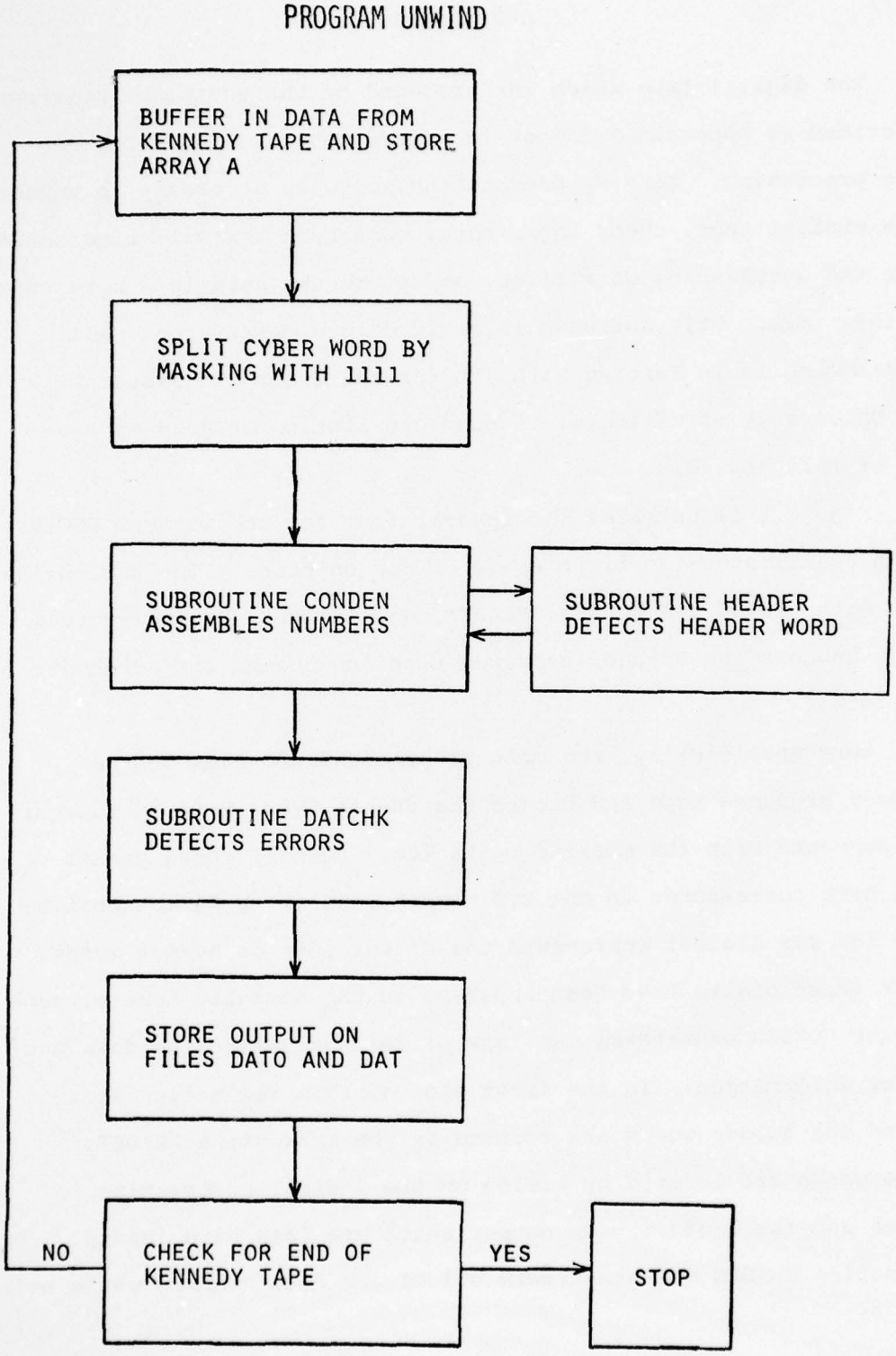


Fig. C.1 Flow for program UNWIND.

routine DATCHK to detect illegal BCD data and sequencing errors. All missing data points are set to the value -99 for easy identification later. Sequencing errors are detected by following the 2-digit frame count in each data word. The unpacked output from the first file on the Kennedy tape is written on file DATO while that of the second file is written on file DAT. Both DATO and DAT are scratch tapes.

The second stage of the program, entitled SERIAL and illustrated in Fig. C.2, reads the intermediate storage files DATO DAT and assembles them into a final time series. Subroutine READF does this reading. Subroutine COLOCAT next determines the skew between the overlapping data files. Once this skew is determined, DATO and DAT are rewound then subroutine COLOCAT produces a single time series. This time series is outputed onto file GHZDAT by subroutine WRITEF every 500 points along with the following

IRECN -- cumulative record number

IDAY -- Julian day

NSTART -- start time of record in seconds

IOBS -- observation number (input)

ICODE -- code number (input)

ICH -- number of channels (input)

NCHAN -- current channel number

ISR -- sample rate (input)

NPTS -- number of data points in record

FREQ -- receiver frequency (input)

LABEL -- 32 character label (input)

DAT -- up to 500 data points

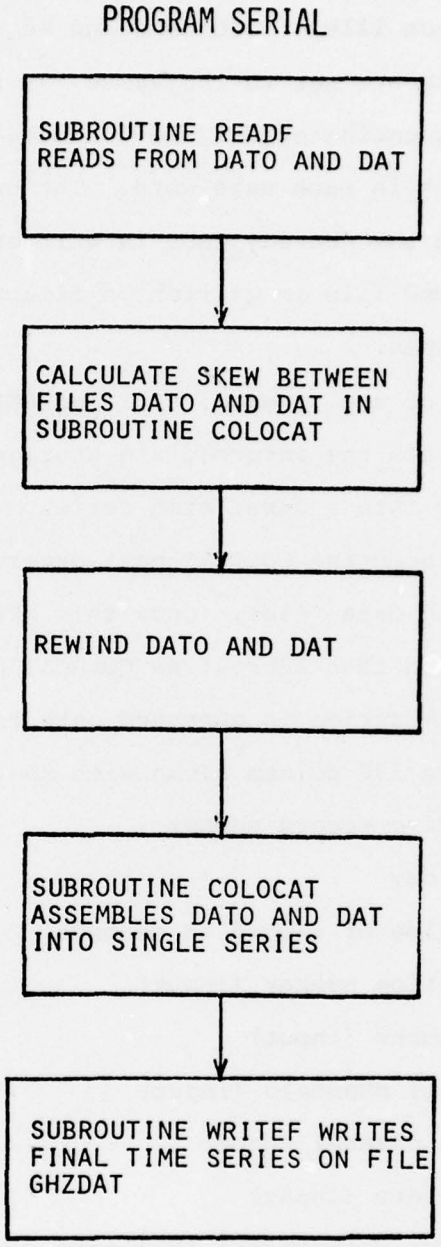


Fig. C.2 Flow for program SERIAL.

where input indicates data is inputed on cards.

The following JCL control these two programs:

```
SIGNON (<ID NO.>)
<PASSWORD>.
BILL, ELEC, PS<PS NO.>.
RESOURC, NT=3.
REQUEST (TDATI, CV=EB, NT, F=L, LB=KU, VSN=GHZ002-E363)
REQUEST (DATO, CV=EB, NT, F=L, LB=KU, VSN=SCRATCH)
REQUEST (DAT, CV=EB, NT, F=L, LB=KU, VSN=SCRATCH)
GET, OUN.
OUN.
RETURN, TDATI, OUN.
REWIND, DATO, DAT.
RESOURC, NT=3.
REQUEST(GHZDAT, CV=EB, NT, F=L, LB=KU, VSN=<tapename>-<rack no.>)
GET, OSER.
789
data set 1
789
data set 2
6789
```

where data set number one consists of 8 cards in the following order:

card no.	variable	format
1	IOBS	I3
2	ICODE	I3
3	ICH	I3
4	MODUP	I3
5	NSKIP	I3
6	ISR	I3
7	JCHAN(I)	8I1
8	LIMIT	I4

where the new quantities are

MODUP = 20

NSKIP = 5

JCHAN(I) = channel number of active data channels. This was introduced to eliminate processing of any unused channels located between good channels.

LIMIT should be greater than 5000 divided by the total number of channels record on the audio tape.

and data set number two consists of up to 10 cards in the following order:

card no.	variable	format
1	LABEL	32A4
2	ICH	I1
3-10	FREQ(I)	F10.3

where FREQ(I) corresponds to the I-1 st data channel; i.e., card three is the frequency for the zeroth channel and card 10 is for the eighth channel.

The object programs OUN and OSER are created by and stored on permanent file by

```
COPYBR,,UNWIND
FTN, I=UNWIND, L=0, OPT=2, B=OUN.
SAVE, OUN.
COPYBR,,SERIAL.
FTN, I=SERIAL, L=0, OPT=2, B=OSER.
SAVE, OSER.
789
     Fortran program UNWIND
789
     Fortran program SERIAL.
6789.
```

```
      PROGRAM UNWIND     74/74   OPT=1 TRACE                    FTN 4.6+439        77/11.

 1          C
            C THIS PROGRAM UNPACKS RAW SCINTILLATION DATA FROM GHZ00- SERIES TAPES
            C
                  PROGRAM UNWIND(INPUT,OUTPUT,TDAT1,TAPE10=TDAT1,DATO,
 5                1TAPE11=DATO,DAT,TAPE12=DAT,TAPE5=INPUT)
                  COMMON/DAT/A(1700),B(1500),DATA(2,2500),IHRR(30),IMINN(30)
                 +,INDE(30),ISAM(10),IDYY(30)
                  COMMON/FLAG/ICH,IOBS,ICODE,LCH,IFC,INDEX,ILOC,IEND,NBEGIN,NLOC,
                 +INDEX1,ISAMP,LOCAT,IDAY,IHR,IMIN,LNOBS,NHEAD,NEXT,MISS
10                ,IFC1,IFC2,MODUP,NSKIP,IFCHK,JCHAN(8),MMISS
                  INTEGER A,B,DATA
                  IFILE=11
            C
            C INDEX1= INDEX VALUE OF PREVIOUS HEADER WORD
15          C LNOBS IS USED TO KEEP INDEX IN RANGE DURING SEARCH FOR HEADER
            C WORDS
            C ITIME KEEPS TRACK OF NUMBER OF ATTEMPTS TO BEAT PARITY
            C ERROR ON BUFFER IN - 3 TRYS ALLOWED
            C
20          C READ IN PARAMETERS FROM CARD INPUT
            C
                  READ(5,100) IOBS
                  NN=0
                  READ(5,100) ICODE
25                READ(5,100) ICH
                  READ(5,100) MODUP
                  READ(5,100) NSKIP
                  READ(5,100) ISR
             100  FORMAT(I3)
30                READ(5,101) (JCHAN(I),I=1,ICH)
             101  FORMAT(8I1)
                  READ(5,102) LIMIT
             102  FORMAT(I4)
            C
35          C BUFFER IN RECORD OF BITS
            C
              3   BUFFER IN(10,1)(A(1),A(1700))
                  IF(UNIT(10)) 1,2,2
            C
40          C CHECK RECORD LENGTH IN WORDS PLUS EXCESS BITS
            C
              1   CALL LENGTHX(10,LN,LUB)
            C
            C  INITIALIZE INDEXES WITH EACH RECORD
45          C
                  ITIME=0
                  NN=NN+1
                  IF(NN.GE.8) GO TO 800
                  INDEX1=0
50                LNOBS=-1
                  INDEX=0
                  IF(EOF(10)) 13,21
             21   CONTINUE
            C
55          C LN=NO. OF 60-BIT WORDS TRANSFERRED
            C LUB=NO. OF UNUSED BITS IN FINAL WORD
            C
```

```
      ILAST=0
      NHEAD=0
60    INDEX2=1
      DO 22 I=1,ICH
      DO 23 J=1,LIMIT
 23   DATA(I,J)=0
 22   CONTINUE
65    C
      C ILAST= INDEX VALUE OF LAST  STOP POINT IN A
      C NHEAD KEEPS TRACK OF NUMBER OF HEADER WORD GROUPS FOUND
      C
      NN=LN-1
70    IF(LUB.EQ.0) NN=LN
      NLOC=1
      DO 10 I=1,NN
      DO 11 J=4,60,4
      C
75    C DO 4-BIT CIRCULAR SHIFTS AND MASK WITH 00...01111
      C
      B(NLOC)=SHIFT(A(I),J)
      B(NLOC)=B(NLOC).AND.15
 11   NLOC=NLOC+1
80    C
      C CONDENSE WORK ARRAY B EVERY 100 WORDS OR 6000 BITS
      C
      IF(I.EQ.NN) GO TO 20
      IF(I-ILAST.LT.100) GO TO 12
85     20   CONTINUE
      ILAST=I
      NLOC=NLOC-1
      CALL CONDEN
      INDEX2=INDEX
90    NLOC=1
 12   CONTINUE
 10   CONTINUE
      C
      C UNPACK LAST PARTIAL WORD
95    C
      IF(LUB.EQ.0) GO TO 4
      NUB=60-LUB
      DO 14 I=4,NUB,4
      B(NLOC)=SHIFT(A(LN),I)
100   B(NLOC)=B(NLOC).AND.15
 14   NLOC=NLOC+1
      NLOC=NLOC-1
      CALL CONDEN
 4    IF(LCH.EQ.1) INDEX=INDEX-1
105   IF(LCH-1) 25,26
 25   LCHT=LCH-1
      DO 24 I=1,LCHT
      IF(DATA(I,INDEX).NE.-99) GO TO 26
 24   CONTINUE
110   DO 27 I=1,ICH
 27   DATA(I,INDEX)=0
      INDEX=INDEX-1
 26   CONTINUE
      WRITE(IFILE,500) INDEX,ICH,NHEAD,IOBS,ICODE,ISR,(INDE(I),IHRR(I),
```



```
115       1IMINN(I),IDYY(I),ISAM(I),I=1,10),IFC1,IFC2,((DATA(I,J),J=1,LIMIT),
          2I=1,ICH)
 500  FORMAT(3014/2814/114(4413/))
      GO TO 3
      C
120   C RETRY BUFFER IN IF PARITY ERROR
      C
 2    ITIME=ITIME+1
      IF(ITIME-2) 15,16
 15   BACKSPACE 10
125   GO TO 3
 16   PRINT 17
 17   FORMAT(1HO,"PARITY ERROR")
 13   IFILE=IFILE+1
      PRINT 501,IFILE
130   501  FORMAT(1X,"END OF FILE",2I,I5)
      IF(IFILE.LT.13) GO TO 3
 800  STOP
      END
```

```
      SUBROUTINE CONDEN
      COMMON/DAT/A(1700),B(1500),DATA(2,2500),IHPE(30),IMISS(30)
     +,INDE(30),ISAM(10),IDYY(30)
      COMMON/FLAG/ICH,IOBS,ICODE,LCH,IPC,INDEX,ILOC,IEND,NBEGIN,NLOC,
     +INDEX1,ISAMP,LOCAT,IDAY,IHR,IMIN,LNOBS,NHEAD,NEXT,MISS
     +,IPC1,IPC2,MODUP,NSKIP,IPCHK,JCHAN(8),MMISS
      INTEGER A,B,DATA
C
C CONDEN SCANS DIGITS IN B, CHECKS FOR BAD DIGITS (GT.9), EXTRACTS TIME
C INFORMATION AND RECONSTRUCTS NUMBERS
C B= DIGIT ARRAY
C NLOC=NO. OF 4-BIT DIGITS IN B
C
C SEARCH FOR HEADER INFORMATION
C
      NBEGIN=1
      CALL HEADER
C
C FIRST TIME THROUGH LOCATE GOOD CHANNEL 0 AS STARTING POINT
C
      NLOCAT=LOCAT+11+6*ICH
      IF(LOCAT.EQ.0) NLOCAT=0
      IF(INDEX.NE.0) GO TO 1
      LCH=ICH
      DO 2 I=1,NLOC,6
      IF(I.GE.LOCAT.AND.I.LE.NLOCAT) GO TO 2
      IF(B(I+3).EQ.0) GO TO 3
    2 CONTINUE
      PRINT 100
  100 FORMAT(1H0,"GOOD CHANNEL 0 NOT FOUND")
      RETURN
    3 NBEGIN=I
      INDEX=1
      LCH=1
    1 MISS=0
      DO 4 I=NBEGIN,NLOC,6
C
C SKIP HEADER AND FOLLOWING SAMPLE
C
      IF(I.GE.LOCAT.AND.I.LE.NLOCAT) MISS=1
      IF(MISS.EQ.1) GO TO 6
C
C CHECK CHANNEL NO. AND FRAME COUNT WITH RUNNING ACCOUNT
C
      ILOC=I
      CALL DATCHK
      IF(MMISS.EQ.1) GO TO 4
      IF(MISS.EQ.1) GO TO 6
C
C MAKE SURE FRAME COUNT AND INDEX CORRESPOND TO INSURE
C THAT ALL POINTS ARE ACCOUNTED FOR
C
      INDEX=IPC-IPCHK
      DATA(LCH,INDEX)=B(I)*100+B(I+1)*10+B(I+2)
      GO TO 9
    6 DATA(LCH,INDEX)=-99
C
```



```
C  INCREMENT CHANNEL NUMBER AND RESET WHEN LCH.GT.ICH
C
    9 LCH1=LCH
      LCH=LCH+1
      IF(LCH.GT.ICH) LCH=1
      IF(LCH.GT.LCH1) GO TO 10
C
C  INCREMENT INDEX AFTER ALL CHANNELS HAVE BEEN ACCOUNTED
C  FOR
C  ADVANCE FRAME COUNT (IPC) WITH INDEX
C
      INDEX=INDEX+1
      IPC=IPC+1
   10 MISS=0
    4 CONTINUE
      RETURN
      END
```

```
      SUBROUTINE HEADER
      COMMON/DATA/A(1700),B(1500),DATA(2,2500),IHRR(30),IMINN(30)
     +,INDE(30),ISAM(10),IDYY(30)
      COMMON/FLAG/ICH,IOBS,ICODE,LCH,IFC,INDEX,ILOC,INBD,NBEGIN,NLOC,
     +INDEX1,ISAMP,LOCAT,IDAY,IHR,IMIN,LNOBS,NHEAD,NEXT,MISS
     +,IFC1,IFC2,MODUP,NSKIP,IPCHK,JCHAN(8),MMISS
      INTEGER A,B,DATA
      LOCAT=0
C
C  INITIALIZE HEADER ARRAYS WITH EACH RECORD
C
      IF(INDEX) 31,32
 32   DO 30 J=1,10
      IDYY(J)=0
      INDE(J)=0
      ISAM(J)=0
      IHRR(J)=0
 30   IMINN(J)=0
 31   CONTINUE
C
C SCAN B FOR PAIR OF HEADER WORDS  KEY ON IOBS AND ICODE
C
      NOBS=LNOBS
      NB=NBEGIN
      IF(LNOBS.EQ.-1 ) NB=NB+6
 14   DO 1 I=NB,NLOC,6
      IF(NBEGIN.EQ.1) GO TO 9
C
C CHECK FOR ILLEGAL BCD DIGITS
C
      DO 2 J=1,3
 2    IF(B(I-7+J).GT.9) GO TO 1
      IF(B(I+4).GT.9.OR.B(I+5).GT.9) GO TO 1
      NOBS=B(I-3)*100+B(I-2)*10+B(I-1)
 9    NCODE=B(I+4)*10+B(I+5)
      IF(IOBS.EQ.NOBS.AND.NCODE.EQ.ICODE) GO TO 3
 1    CONTINUE
      LNOBS=NOBS
      RETURN
C
C  IND IS INDEX VALUE OF HEADER WORD LOCATION
C  ISAMP IS NUMBER OF SAMPLES BETWEEN HEADER WORDS
C
 3    IND=INDEX+1/(6*ICH)
      IF(INDEX.EQ.0) IND=IND+1
      ISAMP=IND-INDEX1
      IF(INDEX1.EQ.0)ISAMP=0
      INDEX1=IND
 21   II=I
C
C CHECK FOR ILLEGAL BCD DIGITS IN DATE AND TIME
C
      LOCAT=I-6
      DO 4 I=1,3
      IF(B(LOCAT+2+I).GT.9) GO TO 5
 4    CONTINUE
      IDAY=B(LOCAT+3)*100+B(LOCAT+4)*10+B(LOCAT+5)
```

SUBROUTINE HEADER 74/74 OPT=1 TRACE FTN 4.6+439 77/

```
      GO TO 6
 5    IDAY=-99
 6    DO 7 I=1,4
 7    IF(B(LOCAT+5+I).GT.9) GO TO 8
      IHR=B(LOCAT+6)*10+B(LOCAT+7)
      IMIN=B(LOCAT+8)*10+B(LOCAT+9)
C
C  SAVE ALL HEADER INFORMATION
C
      NHEAD=NHEAD+1
      IDYY(NHEAD)=IDAY
      ISAM(NHEAD)=ISAMP
      INDE(NHEAD)=IND
      IHRR(NHEAD)=IHR
      IMINN(NHEAD)=IMIN
      IF(II.GE.NLOC-6) GO TO 13
      NB=II
      GO TO 14
 13   RETURN
 8    IHR=-9
      IMIN=-9
      RETURN
      END
```

```
SUBROUTINE DATCHK     74/74   OPT=1 TRACE                    FTN 4.6+439        77/11/18.

 1                SUBROUTINE DATCHK
                  COMMON/DAT/A(1700),B(1500),DATA(2,2500),IHRR(30),IMINN(30)
                 +,INDE(30),ISAM(10),IDYY(30)
                  COMMON/FLAG/ICH,IOBS,ICODE,LCH,IFC,INDEX,ILOC,IEND,NBEGIN,NLOC,
 5               +INDEX1,ISAMP,LOCAT,IDAY,IHR,IMIN,LNOBS,NHEAD,NEXT,MISS
                 +,IFC1,IFC2,MODUP,NSKIP,IFCHK,JCHAN(8),MMISS
                  INTEGER A,B,DATA
               C
               C THIS SUBROUTINE COMPARES RUNNING ACCOUNT OF CHANNEL NO. AND FRAME COUNT
10             C WITH VALUE ON TAPE TO CHECK FOR MISSING DATA AND ALSO CHECKS FOR
               C ILLEGAL DATA
               C
               C LCH=RUNNING CHANNEL NO.
               C IFC=RUNNING FRAME COUNT
15             C INDEX=LOCATION IN ARRAY DATA
               C MISS=0 FOR GOOD DATA POINT
               C      =1 FOR MISSED POINT
               C
                      IMISS=0
20                    DO 1 J=1,3
               C
               C CHECK DATA FOR ILLEGAL BCD DIGITS
               C
                1     IF(B(ILOC+J-1).GT.9) MISS=1
25                    IF(MISS.EQ.1) RETURN
               C
               C COMPARE RUNNING CHANNEL NO. WITH VALUE IN DATA WORD
               C
                      MMISS=0
30                    MCH=B(ILOC+3)
                      DO 30 M=1,ICH
                      IF(MCH.EQ.JCHAN(M)) GO TO 31
                 30   CONTINUE
                      MMISS=1
35                    RETURN
                 31   NCH=M-1
                 32   CONTINUE
               C
               C  RUNNING CHANNEL NUMBER NCH MUST BE .LT. NO. OF CHANNELS
40             C  SELECTED (ICH-1)
               C
                      IF(NCH.GT.ICH-1) MISS=1
                      IF(MISS.EQ.1) RETURN
                      IF(NCH-LCH+1) 2,3,4
45              4     DATA(LCH,INDEX)=-99
               C
               C IF RUNNING ACCOUNT AND RECORDED VALUE DISAGREE
               C
                2     IMISS=1
50             C
               C IF CHANNEL NO. OK
               C
                3     CONTINUE
               C
55             C COMPARE FRAME COUNTS
               C
                      IF(B(ILOC+4).GT.9.OR.B(ILOC+5).GT.9) MISS=1
```

SUBROUTINE DATCHK 74/74 OPT=1 TRACE FTN 4.6+439 77/11/18.

```
      IF(MISS.EQ.1) RETURN
      MFC=B(ILOC+4)*10+B(ILOC+5)
60    IF(INDEX-1) 21,20
C
C  INITIALIZE IFC AND IFC1 AT INDEX=1
C
 20   IFC=MFC
65    IFC1=IFC
      IFCHK=IFC1-1
 21   MTRUNK=IFC/100
      MFC=MFC+MTRUNK*100
C
70    C  CHECK FOR RESET OF RELATIVE FRAME COUNT MFC TO 00
C
      IF(MFC.LT.IFC-MODUP) LFC=MFC+(MTRUNK+1)*100
      IF(LFC.EQ.IFC) MFC=LFC
C
75    C  IF ABSOLUTE FRAME COUNT MFC STILL .LT. IFC, SKIP
C
      IF(MFC.LT.IFC) GO TO 23
      IF(MFC-NSKIP.LT.IFC) GO TO 22
 23   MISS=1
80    22   IF(MISS.EQ.1) RETURN
      MFC1=MFC
      MFC2=IFC
C
C  IF FRAME COUNTS AGREE, FRAME IS OK FOR THAT CHANNEL
85    C
 9    IF(MFC.EQ.MFC2) GO TO 5
C
C IF RUNNING VALUE AND RECORDED FRAME COUNT DISAGREE
C FILL IN MISSING FRAMES WITH -99
90    C
      DO 13 J=LCH,ICH
 13   DATA(J,INDEX)=-99
      INDEX=INDEX+1
      IF(MFC-MFC2.EQ.1)GO TO 14
95    NXFC=MFC-1
      DO 12 K=MFC2,NXFC
      DO 10 J=1,ICH
      DATA(J,INDEX)=-99
 10   CONTINUE
100   12   INDEX=INDEX+1
 14   CONTINUE
      IFC=MFC
 5    IF(IMISS.EQ.0) GO TO 7
      IF(NCH.EQ.0) GO TO 7
105   DO 11 K=1,NCH
 11   DATA(K,INDEX)=-99
 7    CONTINUE
      LCH=NCH+1
      IFC2=IFC
110   RETURN
      END
```

```
      PROGRAM SERIAL     74/74   OPT=2                    FTN 4.6+433        77/09/2

      1               PROGRAM SERIAL(INPUT,OUTPUT,DAT3,TAPE1=DAT3,DAT,TAPE2=
                     1DAT,SHZDAT,TAPE4=SHZDAT,TAPE5=INPUT)
                      COMMON/DATBF/DATA(2,2,2500),IFDS(2,10),ISHP(2,10),IMISM(2,
                     110),ISAM(2,10),IDYY(2,10)
      5               COMMON/PARAM/IFILE,ISET,ICH,IOBS,ICODE,ISA,INDSA(2,100),NWID(
                     12),IFC1(2),IFC2(2),IBOF(2),NREC(2),IEF
                      COMMON/OUT/DAT(8,1000),NOUT,NSTART,IBECN,NPTS,NCHAN,IBFD(8),
                     1LABEL(32),IDAY
                      INTEGER DATA,XSAM,DAT
      10              NREC(1)=0
                      NREC(2)=0
                      IBOF(1)=0
                      IBOF(2)=0
                C
      15        C READ IN LABEL AND FREQUENCIES FROM CARD INPUT
                C
                      READ(5,103) (LABEL(I),I=1,8)
                103   FORMAT(4A4,4A4)
                      READ(5,102) ICH,(FREQ(I),I=1,ICH)
      20        102   FORMAT(I2/8(F10.3/))
                C
                C  READ IN DATA UNTIL SET WITH HEADER WORD IS LOCATED
                C
                      IFILE=1
      25              ISET=1
                4     CALL READF
                      IF(IBOF(ISET)) 9,3
                2     IF(NHEAD(ISET)) 3,4
                3     CONTINUE
      30        C
                C  READ IN DATA FROM OVERLAPPING FILE UNTIL HEADER WORD
                C  IS LOCATED
                C
                      IFILE=2
      35              ISET=2
                7     CALL READF
                       IF(IBOF(ISET)) 9,5
                5     IF(NHEAD(ISET)) 6,7
                6     CONTINUE
      40              IER=0
                      CALL COLOCAT
                      IF(IER.EQ.0) GO TO 8
                      GO TO 8
                9     PRINT 100,IFILE
      45        100   FORMAT(1H0///,"/////  NO HEADER WORD FOUND ON FILE NUMBER ",
                     1I2," /////"////)
                      GO TO 8
                9     PRINT 101
                101   FORMAT(1H0,///"////ALIGNMENT ERROR ON OVERLAPPING FILES////"///)
      50        8     CONTINUE
                      STOP
                      END
```

```
SUBROUTINE READF      74/74   OPT=2                    FTN 4.6+438      77/09/2

1                     SUBROUTINE READF
                      C
                      C THIS SUBROUTINE READS FROM INTERMEDIATE FILE STORAGE
                      C
5                     COMMON/DATES/DATA(2,2,2500),INDX(2,10),IHRP(2,10),IMIN(2, 0),
                     1ISPM(2,10),IDYY(2, 0)
                      COMMON/PARAM/IFILE,ISET,ICH,IOPS,ICODE,ISP,INDEX(2,100),NHEAD(2),
                     1IPC1(2),IPC2(2),IADF(2),NPTC(2),IBI
                      INTEGER DATA
0                     M=NPTC(ISET)+1
                      READ(IFILE,100) INDEX(ISET,M),ICH,NHEAD(ISET),IOPS,ICODE,ISP,
                     1((INDX(ISET,I),IHRP(ISET,I),IMIN(ISET,I),ISPM(ISET,I),
                     2IDYY(ISET,I),I=1,10),IPC (ISET),IPC2(ISET),((DATA(ISET,I,J)
                     3,J=1,2500),I=1,ICH)
5               100   FORMAT(3014/(6E14/ 4(4E13/))
                      IF(EOF(IFILE)) 2,1
                1     NPTC(ISET)=NPTC(ISET)+1
                      RETURN
                2     IPOF(ISET)=1
0                     RETURN
                      END
```

```
SUBROUTINE COLOCAT    74/74   OPT=2                    FTN 4.6+434      77/04/2

      1               SUBROUTINE COLOCAT
                      C
                      C THIS SUBROUTINE DETERMINES THE SKEW BETWEEN THE TWO INPUT FILES
                      C AND CREATES ONE CONTINUOUS DATA STRING
      5               C
                            COMMON/DATBP/DATA(2,2,3500),INDX(2,10),IHRP(2,10),IMIN(2,10),
                           1ISAM(2,10),IDYY(2,10)
                            COMMON/PARAM/IFILP,ISET,ICH,IUBS,ICODE,ISR,INDEX(2,100),NHEAD(2),
                           2IFCT(2),IFC2(2),IEOF(2),NREC(2),IRB
                     10     DIMENSION MBACK(2),IBACK(2)
                            COMMON/OUT/DAT(8,1000),NOUT,NSTART,IBEGN,NPTS,NCHAN,FREQ(2),
                           3LABEL(32),IDAY
                            INTEGER DATA,XSAM,DAT
                            XSAM=ISR/2
                     15     IDAY=IDYY(1,1)
                      C
                      C  DETERMINE ABSOLUTE TIME OF FIRST POINT IN FIRST RECORD OF
                      C  EACH FILE
                      C
                     20     MBACK(1)=INDX(1,1)
                            MBACK(2)=INDX(2,1)
                            DO 1 I=1,2
                            NR=NREC(I)-1
                            IF(NR.LE.0) GO TO 4
                     25     DO 2 J=1,NR
                          2 MBACK(I)=MBACK(I)+ISAM+INDEX(I,NREC(I)-J)
                          4 X=MBACK(I)
                            Y=ISR
                          1 IBACK(I)=X/Y
                     30     DO 3 I=1,2
                            IHR=IHRP(I,1)
                            IF(IHRP(I,1).LT.24) IHR=IHRP(I,1)+24
                          3 IBACK(I)=IHR*3600+IMIN(I,1)*60-IBACK(I)
                            NSTART=IBACK(1)
                     35     IF(NSTART.GE.86400) NSTART=NSTART-86400
                      C
                      C  REWIND FILES
                      C
                            REWIND 1
                     40     REWIND 2
                      C
                      C  READ IN FIRST RECORDS
                      C
                            IFILP=1
                     45     ISET=1
                            CALL READF
                            IFILP=2
                            ISET=2
                            CALL READF
                     50     C
                      C  CALCULATE SKEW BETWEEN RECORDS
                      C
                            ISKEW=(IBACK(2)-IBACK(1))*ISR
                      C
                     55     C  CORRECT SKEW TO MATCH FRAME COUNTS
                      C
                            MIFUNK=ISKEW/100
```

```
 SUBROUTINE COLOCAT    74/74   OPT=2                    FTN 4.6+439      77/03/

                MTRUNK=MTRUNK*100
                MFC=ISKEW-MTRUNK
 50             NSKEW=IFC1(2)-IFC1(1)
                IF(NSKEW.LT.0) NSKEW=NSKEW+100
                IER=0
                NABS=IABS(MFC-NSKEW)
                IF(NABS.LT.NREC(1)+NREC(2)+5) GO TO 5
 55        C
           C ABORT IF ALIGNMENT IS UNREASONABLE
           C
                IER=1
                RETURN
 70         5   NREC(1)=1
                NREC(2)=1
                NSKEW=MTRUNK+MFC
                NPTS=0
                INDEX1=0
 75             INDEX2=0
           C
           C  USE FILE 11 AS BASIS
           C
                ISET=1
 80             NSK=1
                IRETURN=0
              2 DO 3 J=NSK,NSKEW
                NPTS=NPTS+1
                DO 7 I=1,ICH
 85           7 DAT(I,NPTS)=DATA(ISET,I,J)
                IF(NPTS-500) 8,24,8
             24 IRETURN=1
                GO TO 29
              8 INDEX1=INDEX1+1
 90           18 IRETURN=0
                NPTS=NPTS+1
                DO 9 I=1,ICH
                IF(INDEX1+1) 10,10,11
             11 DAT(I,NPTS)=DATA(1,I,INDEX1+1)
 95             IF(INDEX2+1) 9,9,13
             13 IF(DAT(I,NPTS).LE.J) DAT(I,NPTS)=DATA(2,I,INDEX2+1)
                GO TO 9
             10 DAT(I,NPTS)=DATA(2,I,INDEX2+1)
              9 CONTINUE
100             INDEX1=INDEX1+1
                INDEX2=INDEX2+1
                IF(NPTS-500) 23,19
             19 NSK=J+1
                DO 20 K=1,ICH
105             NCHAN=K-1
                IRECN=IRECN+1
           C
           C WRITE OUTPUT ON TAPE
           C
110          20 CALL WRITEF
                NSTART=NSTART+500/ISR
                DO 29 II=1,500
                DO 29 IJ=1,ICH
             29 DAT(IJ,II)=0
```

```
      SUBROUTINE COLOCAT    74/74   OPT=2                    FTN 4.6+436    77/09/
      IF(IRETURN-1) 26,27
   27 INDEX1=INDEX1+1
      NPTS=0
      IF(NSK.LE.NSKEW) GO TO 28
      GO TO 18
   26 IF(IBUF(2).EQ.1) RETURN
      NPTS=0
   23 IF(INDEX1-INDEX(1,1)) 25,15,15
   25 IF(INDEX2-INDEX(2,1)) 18,16,16
   16 ISET=2
      IFCOLD=IFC2(2)-(IFC2(2)/100)*100
      IFILE=12
      NREC(2)=0
      CALL READF
      IF(IBUF(2).EQ.1) GO TO 19
      INDEX2=IFCOLD-IFC1(2)
      IF(INDEX2.GE.0) INDEX2=INDEX2- 00
      GO TO 18
   15 ISET=1
      IFCOLD=IFC2(1)-(IFC2(1)/100)*100
      IFILE=11
      NREC(1)=0
      CALL READF
      IF(IBUF(1)-1) 21,22
   22 INDEX1=-5000
      GO TO 18
   21 INDEX1=IFCOLD-IFC1(1)
      IF(INDEX1.GE.0) INDEX1=INDEX1- 00
      GO TO 18
      END
```

```
      SUBROUTINE WRITEF     74/74   OPT=2                    FTN 4.6+436    77/09/0
            SUBROUTINE WRITEF
      C
      C THIS SUBROUTINE WRITES FINAL OUTPUT ON TAPE
      C
            COMMON/PARAM/IFILE,ISET,ICH,ICBS,ICODE,ICH,INDEX(2,100),NREAD(2)
           1,IFC1(2),IFC2(2),IBUF(2),NREC(2),IAR
            COMMON/OUT/DAT(8,5000),IOUT,NSTART,IBEGN,NPTS,NCHAN,PERO(8),
           1LABEL(32),IDAY
            INTEGER DAT
            NOUT=14
            ICHAN=NCHAN+1
            WRITE(NOUT, 00) IBEGN,IDAY,NSTART,ICBS,ICODE,ICH,NCHAN,IAR,NPTS,
           1PERO(ICHAN),(LABEL(I),I=1,4),((DAT(ICHAN,I),I=1,5000)
        100 FORMAT(9I5,2X0.2,4A4/(8(4013/))
            RETURN
            END
```

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